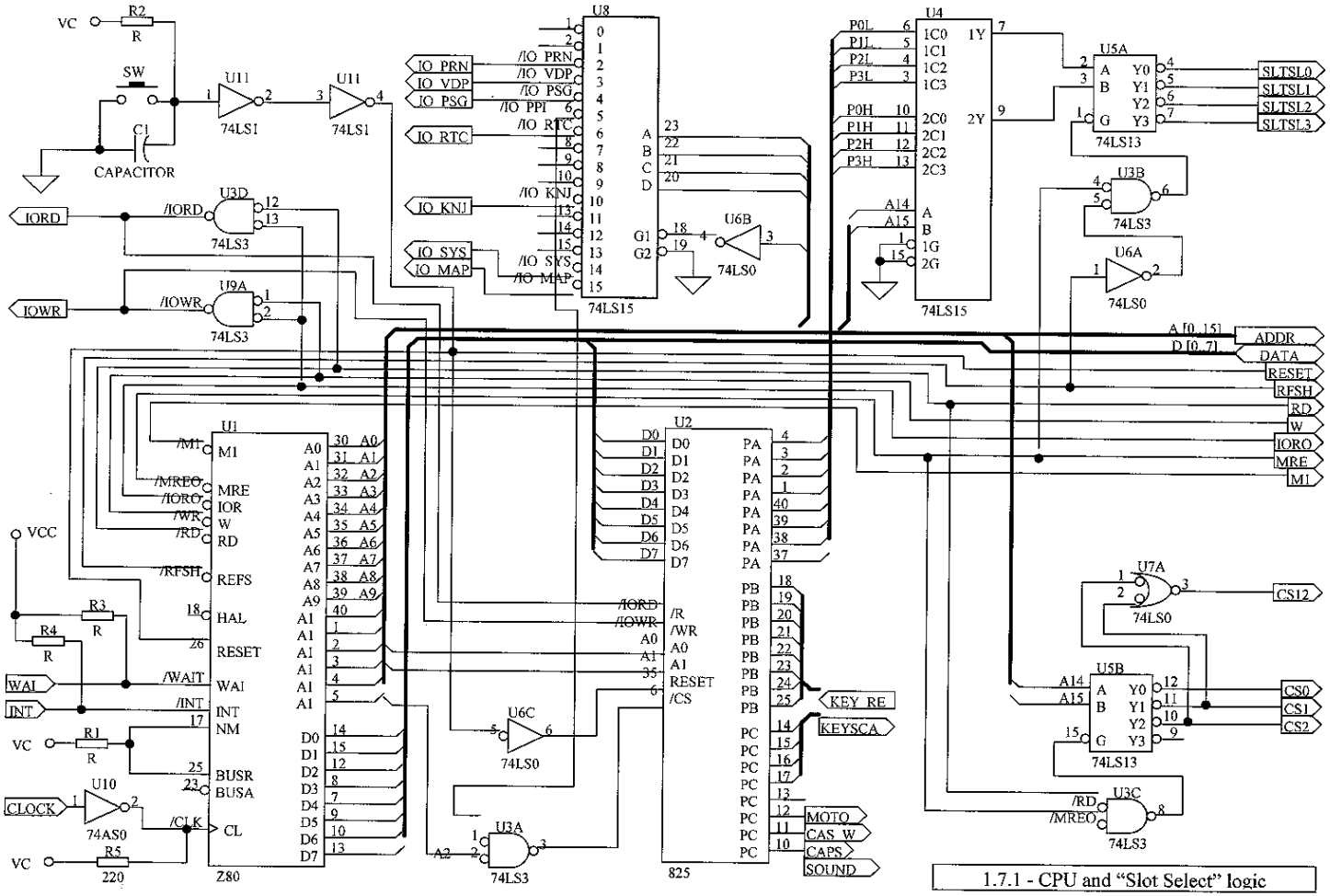
From "MSX Datapack Volume 1", ASCII Co., Japan
By "Cyberknight" Massao Kawata

Hardware MSX2+.

Notas do tradutor

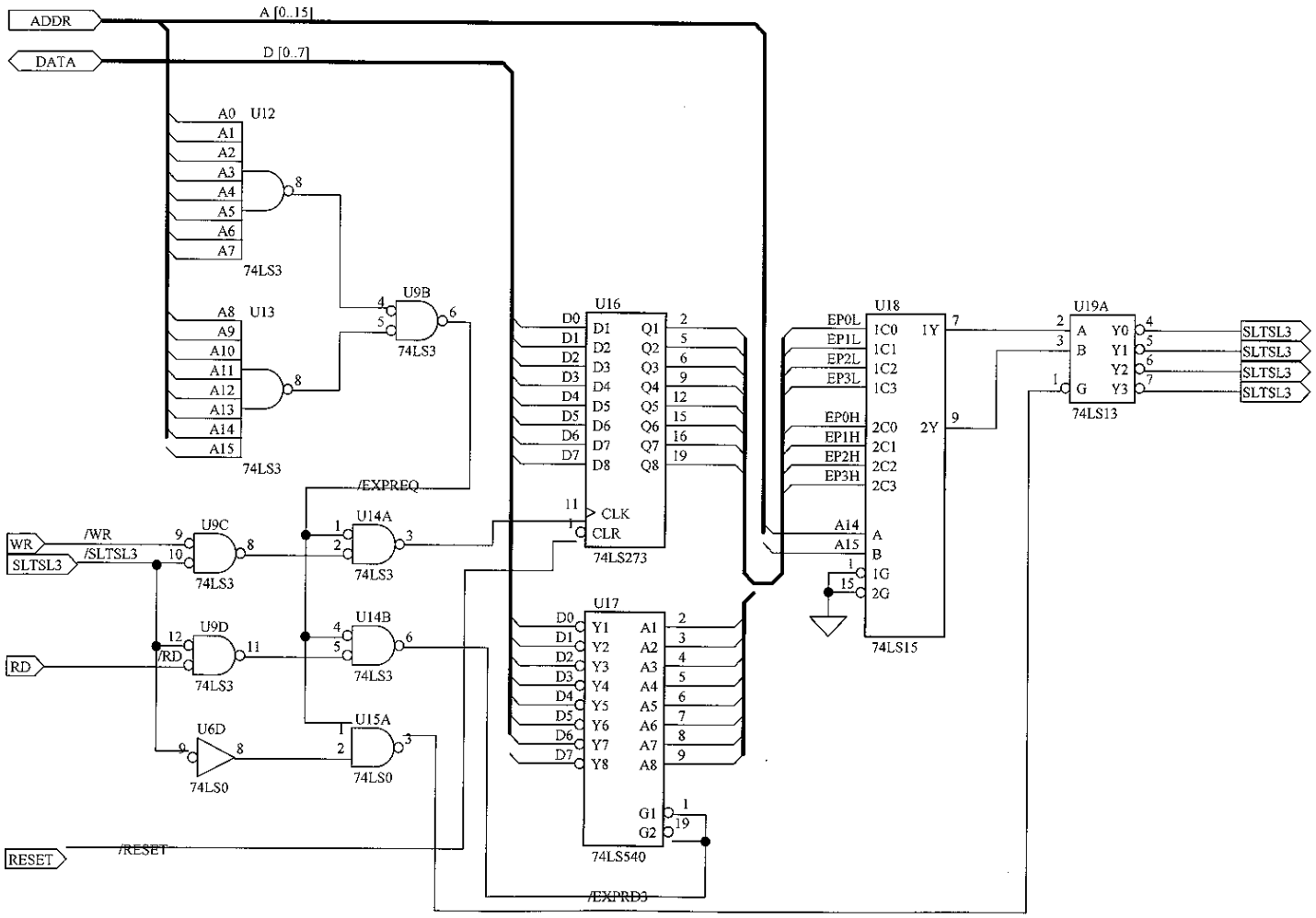
1 - CPU and "Slot Select logic
2 - Expanded Slot Select logic;
3 - System Control Port
4 - System ROM
5 - Main RAM
6 - VDP
7a - PSG
7b - System Wait logic
8 - Kanji ROM
9 - Printer Interface
10 - Real Time Clock
11 - Cartridge Slot
* - Memory Mapper

Converted to PDf by HansO, 2001

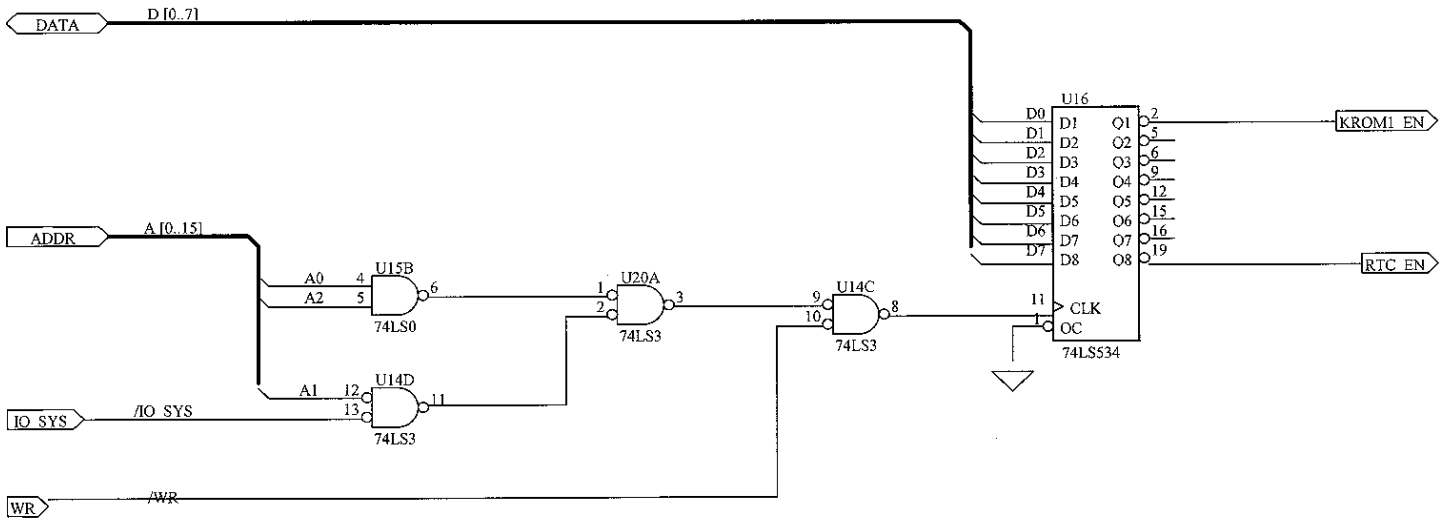


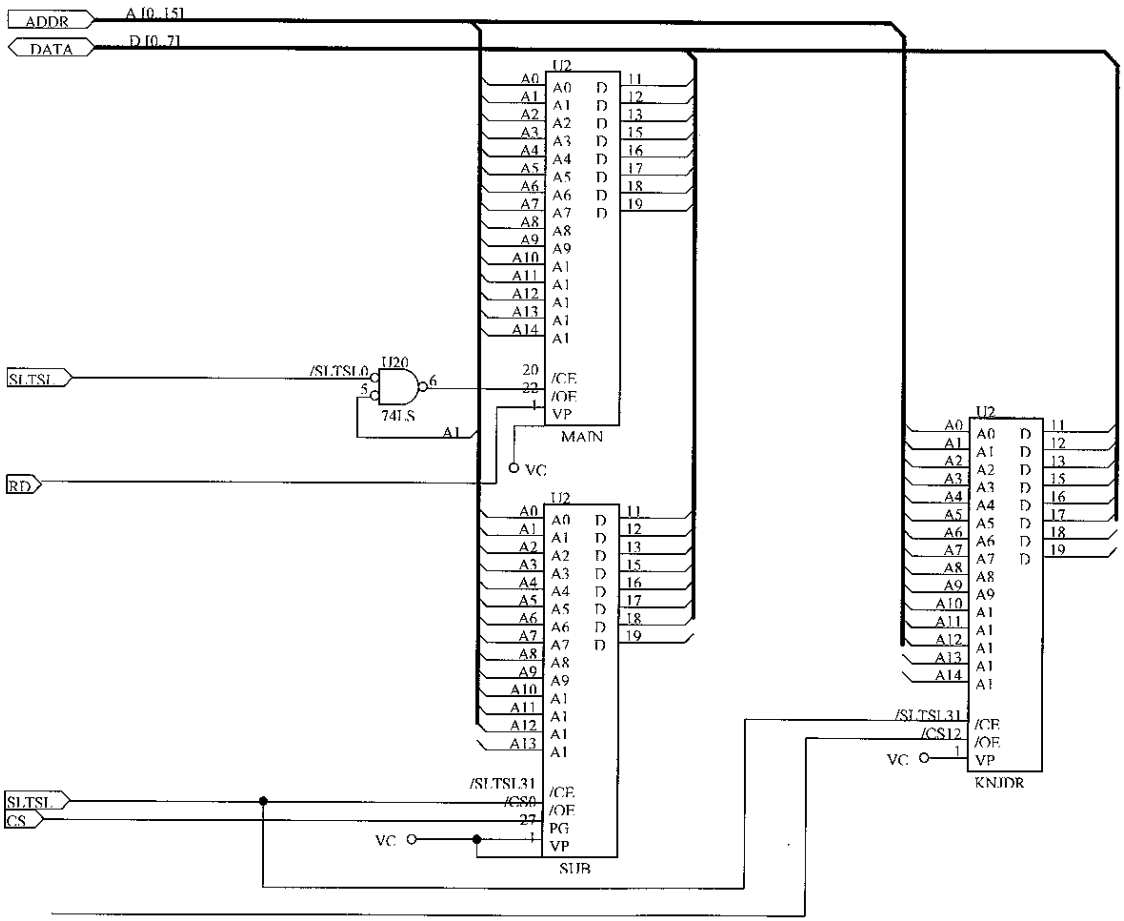
1.7.1 - CPU and "Slot Select" logic

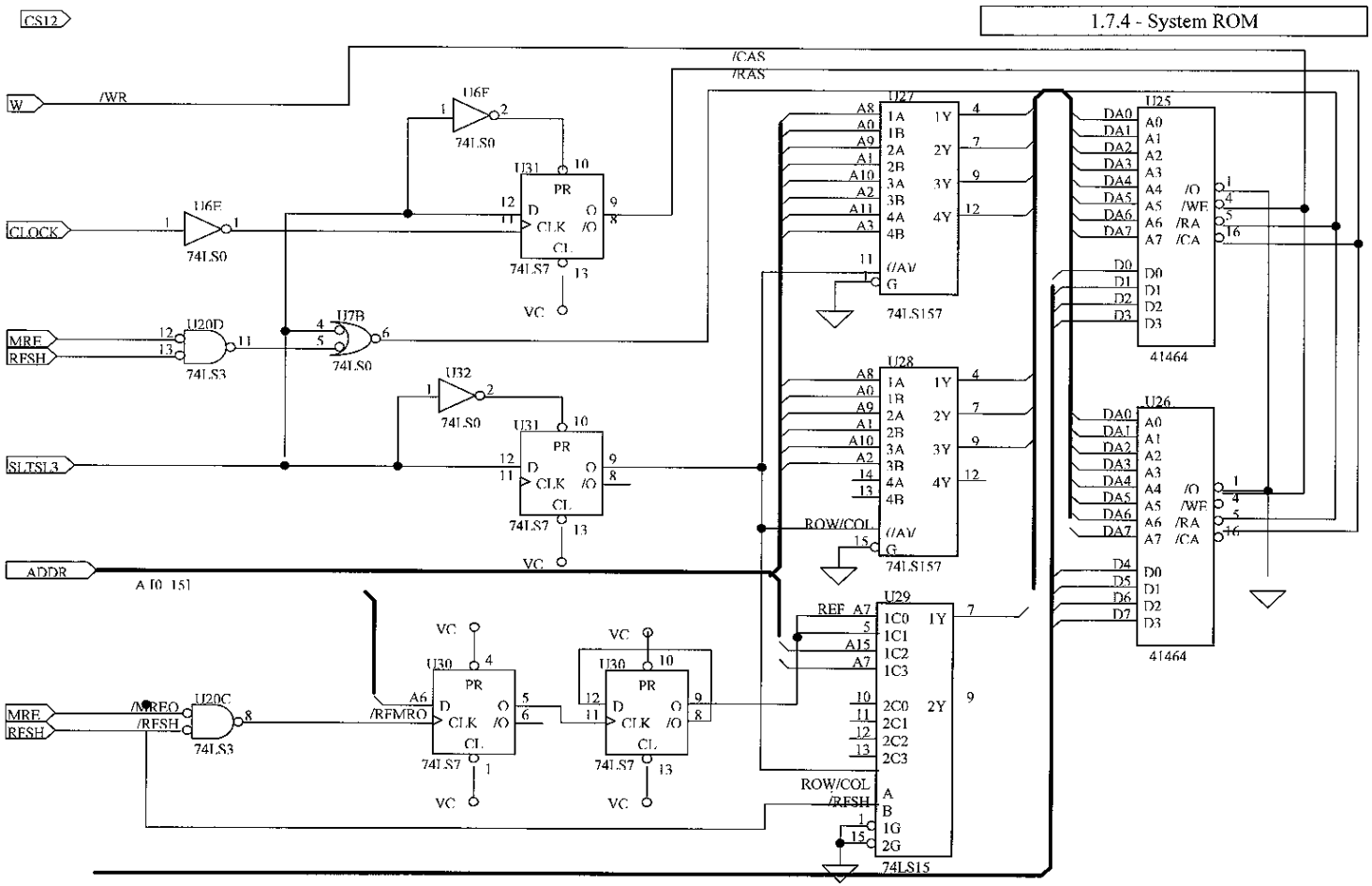
1.7.2 - "Expanded Slot Select" logic

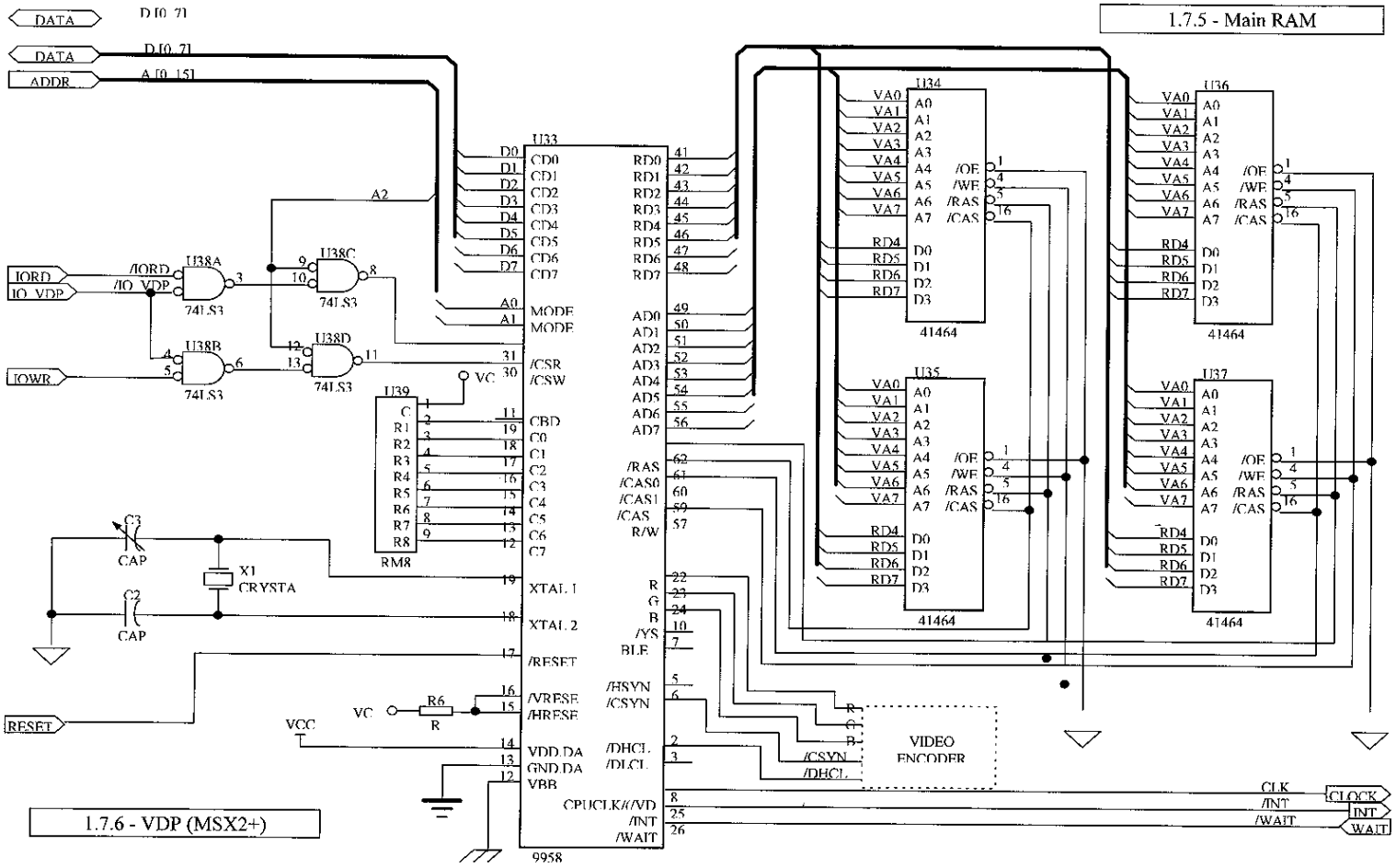


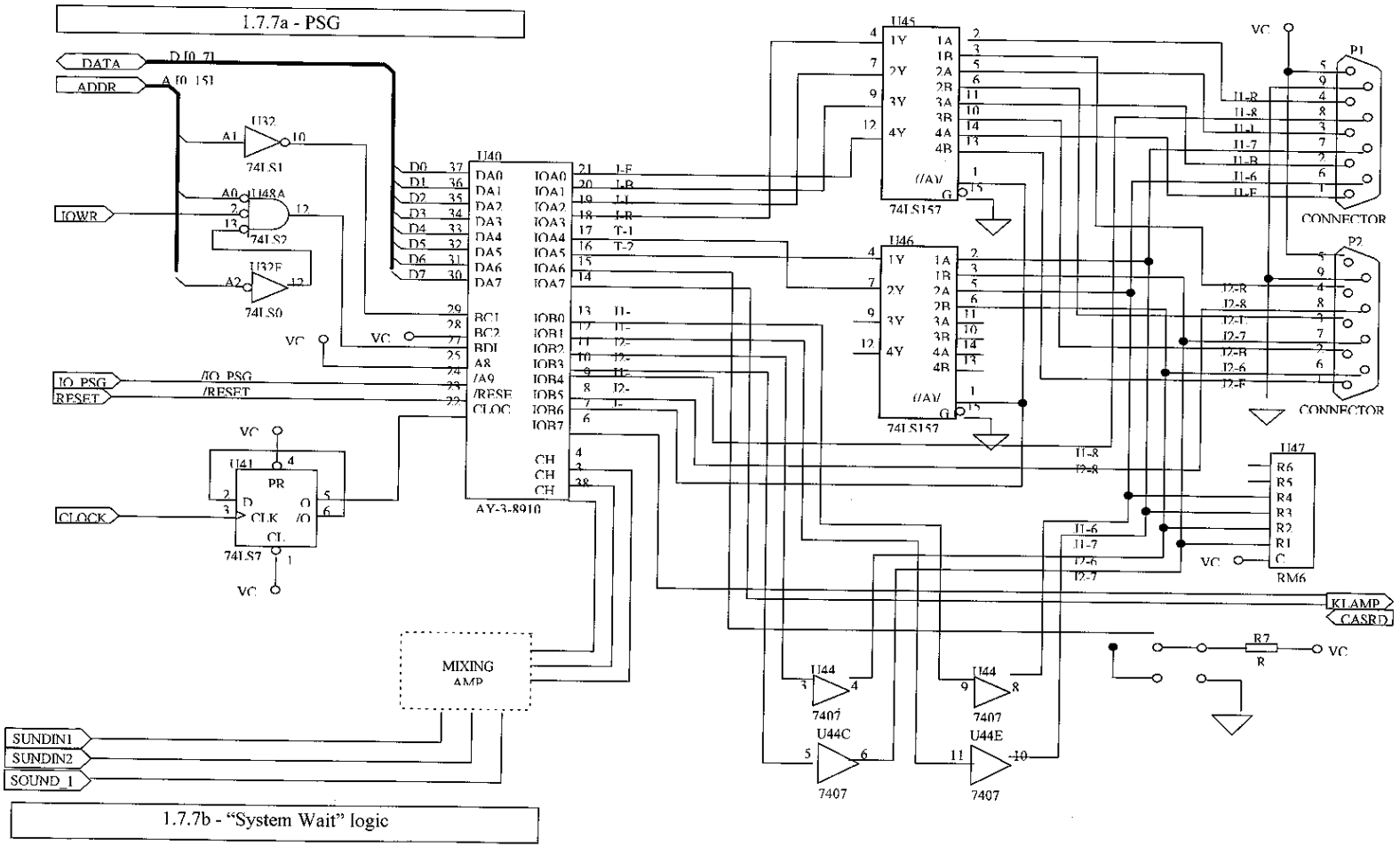
1.7.3 - System Control Port

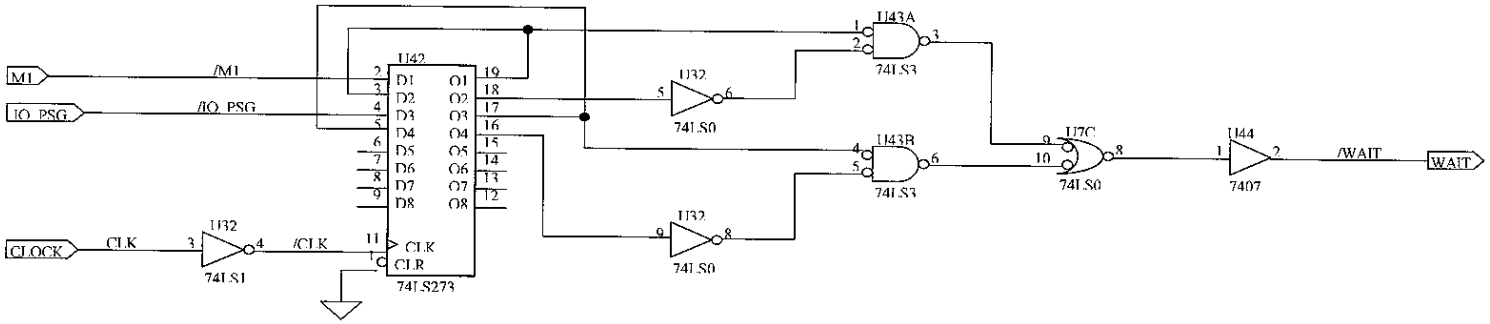


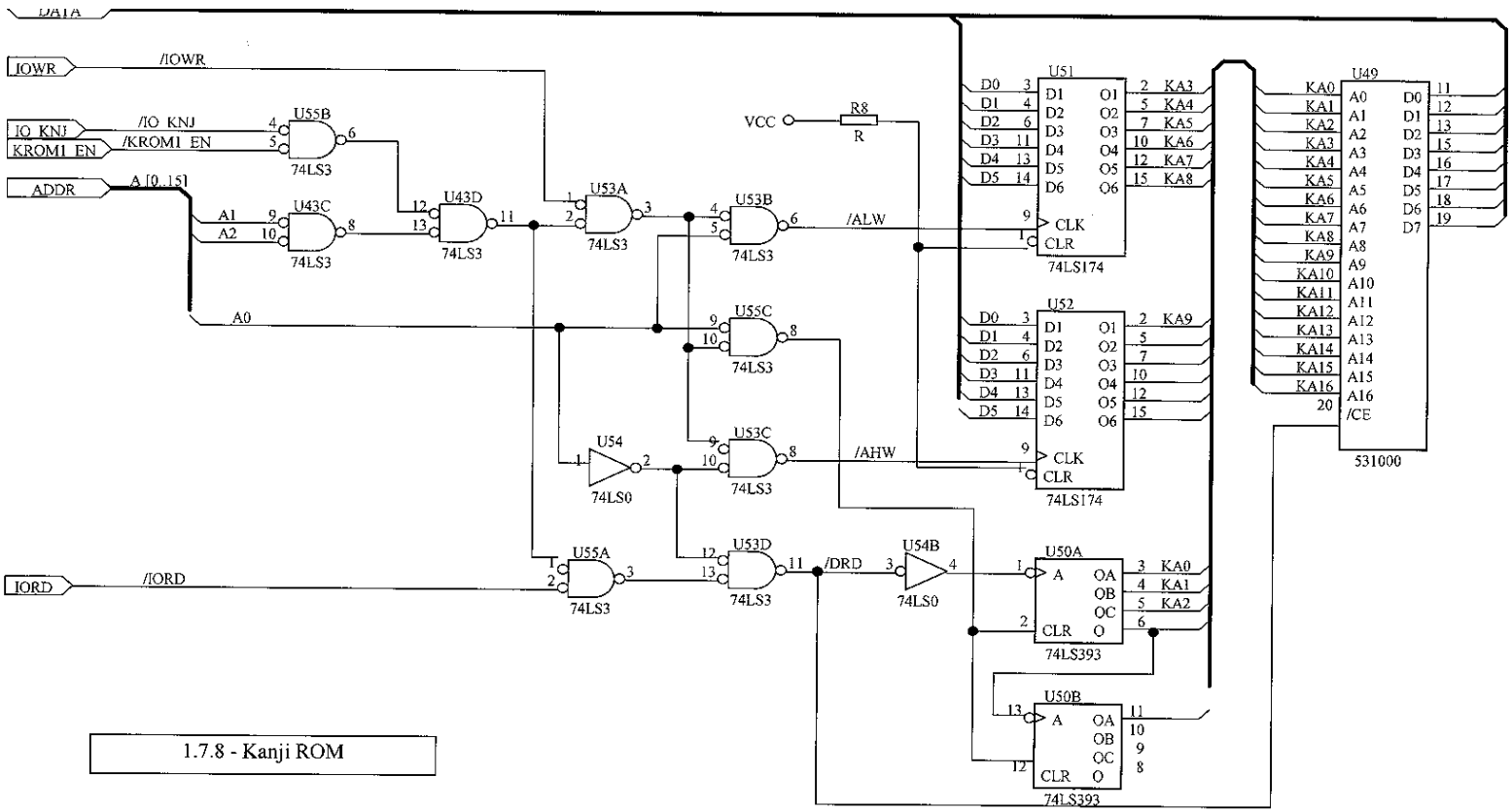

ADDR
A[0..15]
DATA
D[0..7]
U2
MAIN
SUB
KNJDR
U20
74LS
SLTSL
/SLTSL0
/SLTSL31
/CS12
RD
CS
VC
/CE
/OE
VP
PG


1.7.4 - System ROM
CS12
W
/WR
/CAS
/RAS
CLOCK
MRE
RFSH
SLTSL3
ADDR
A [0..15]
U6F
U6E
U20D
U7B
U32
U31
U30
U20C
74LS0
74LS3
74LS7
PR
D
CLK
CL
/O
VC
/MREQ
/RFSH
/RFMRQ
U27
U28
U29
U25
U26
74LS157
74LS15
41464
ROW/COL
REF
/WE
/RA
/CA
DA0
DA1
DA2
DA3
DA4
DA5
DA6
DA7
D0
D1
D2
D3
D4
D5
D6
D7

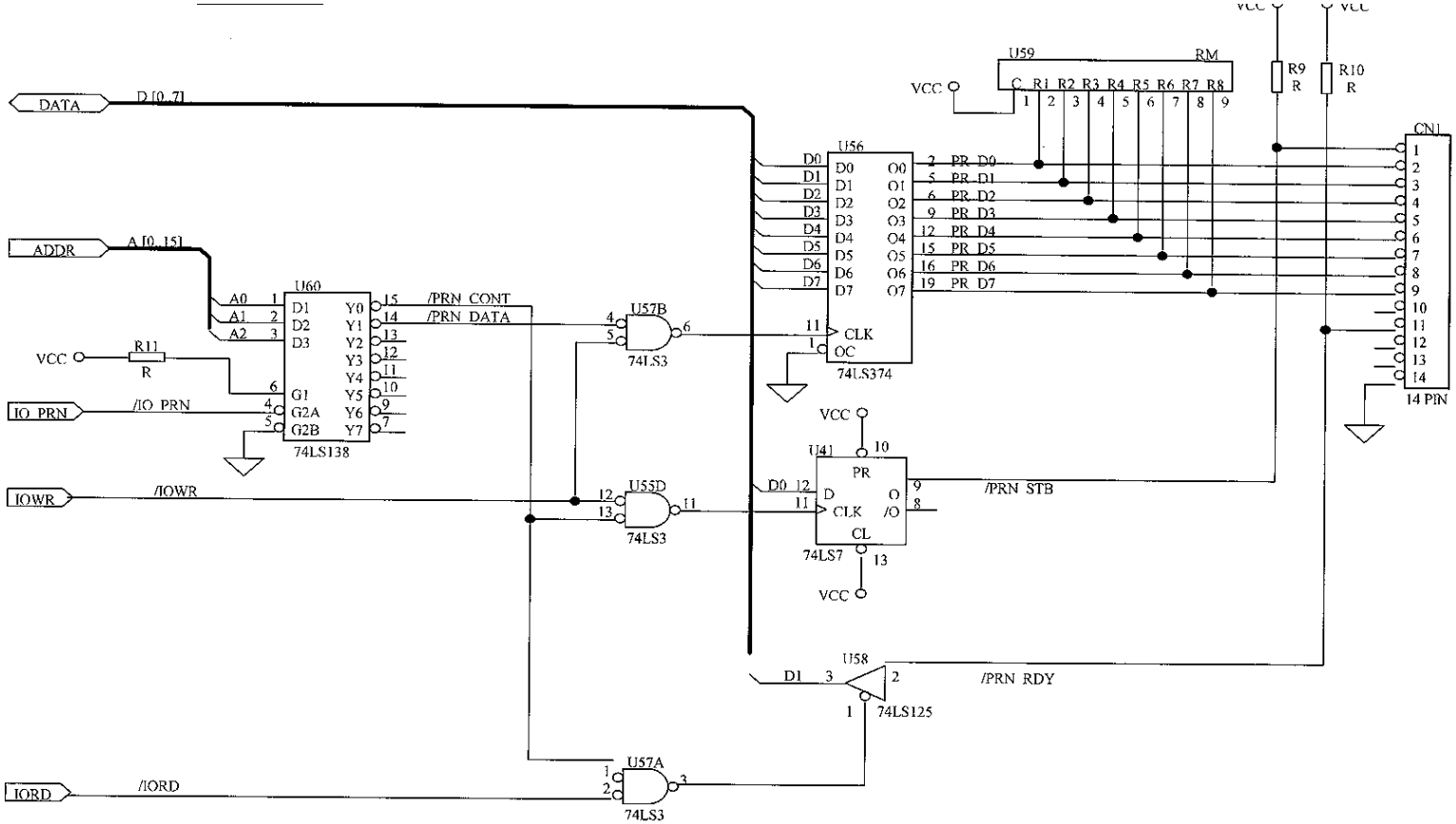

1.7.5 - Main RAM
1.7.6 - VDP (MSX2+)
DATA
ADDR
IORD
IO_VDP
IOWR
RESET
U33
9958
U34
U35
U36
U37
41464
U38A
U38B
U38C
U38D
74LS3
U39
RM8
X1
CRYSTA
C3
C2
CAP
R6
R
VCC
VC
VIDEO
ENCODER
CLK
/INT
/WAIT
CLOCK
INT
WAIT

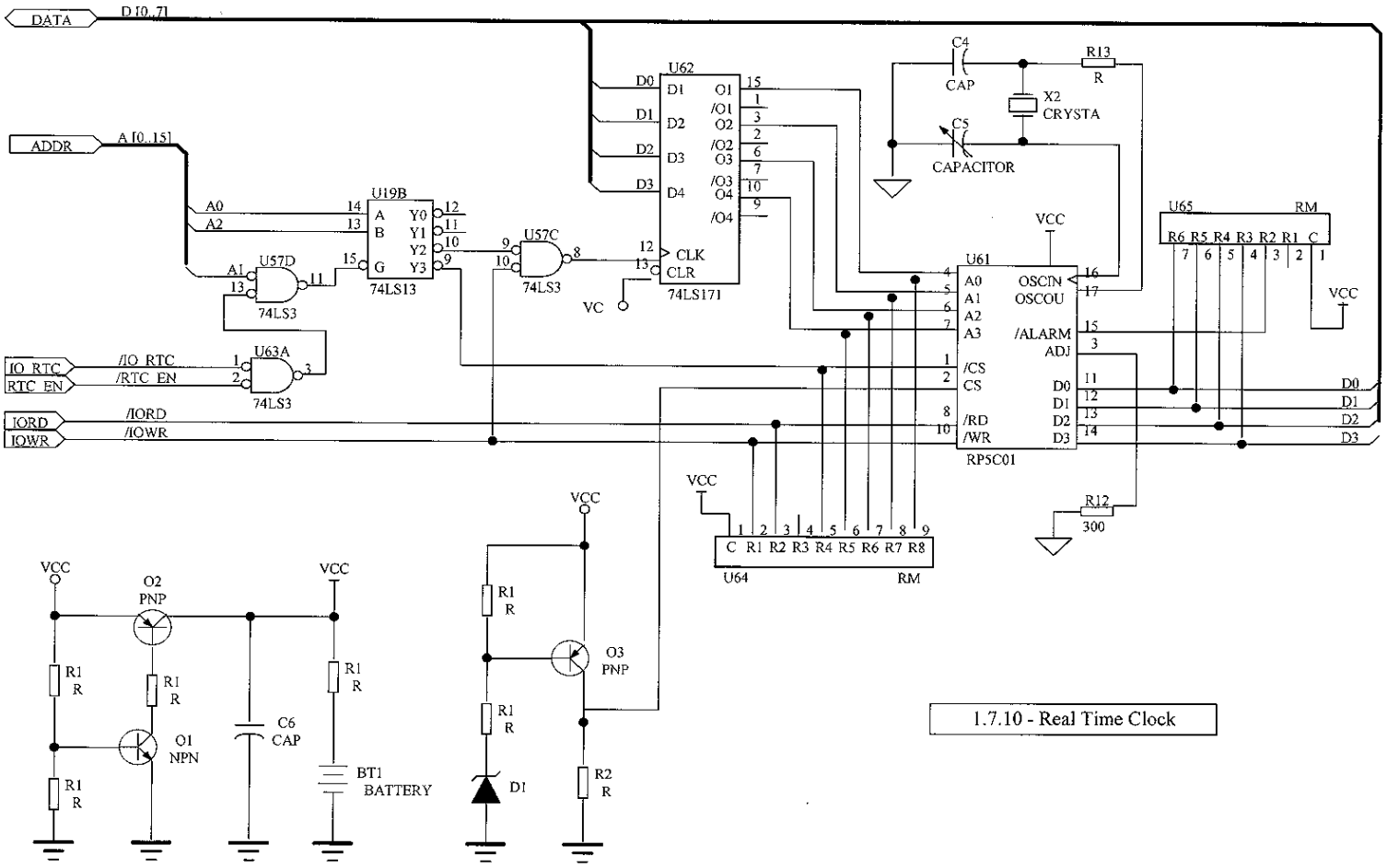

1.7.7a - PSG
DATA
ADDR
IOWR
/IO_PSG
/RESET
CLOCK
MIXING AMP
SUNDIN1
SUNDIN2
SOUND_1
AY-3-8910
74LS157
74LS157
CONNECTOR
CONNECTOR
RM6
KLAMP
CASRD
7407
7407
7407
7407
1.7.7b - "System Wait" logic

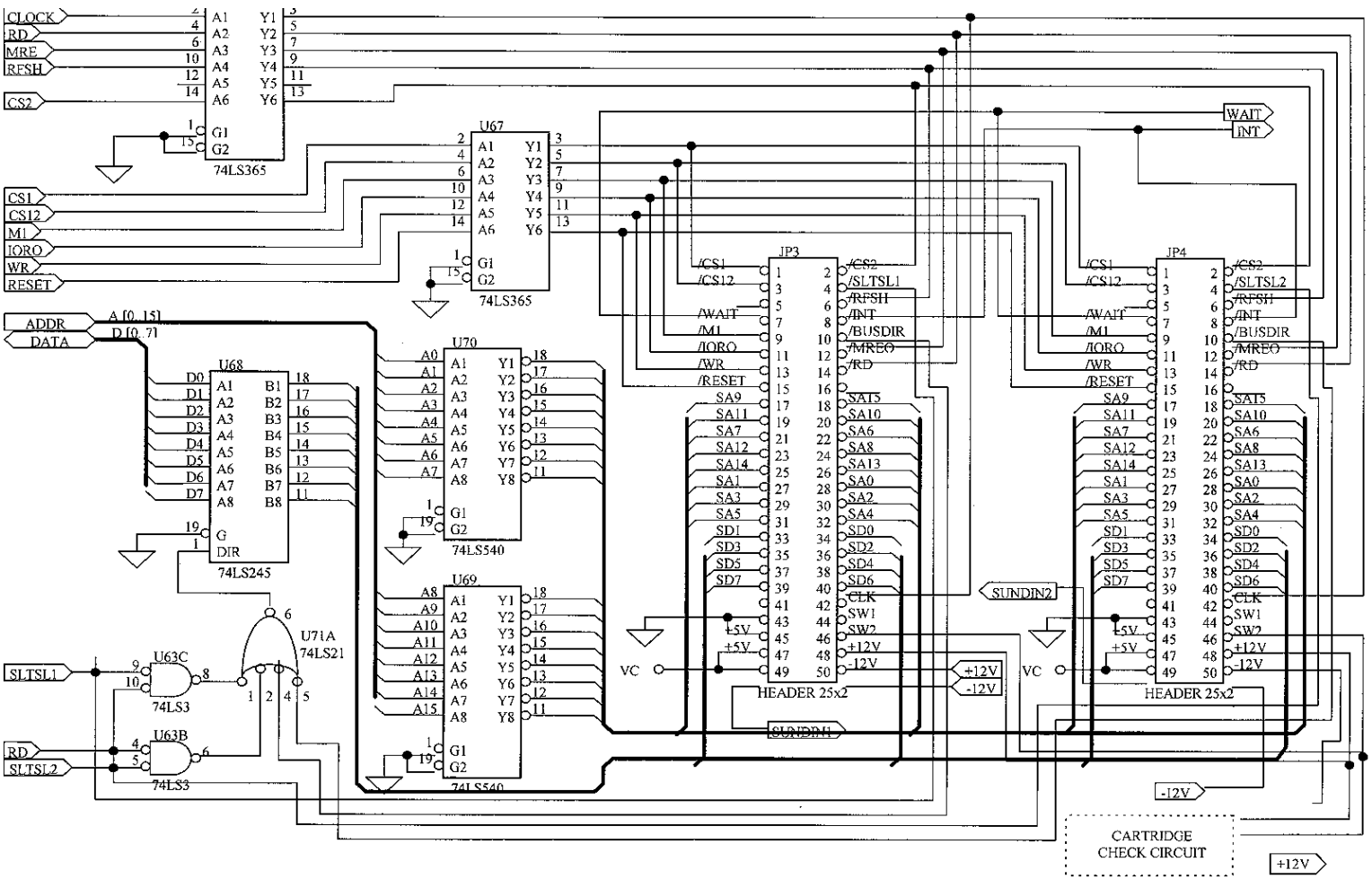

M1
/M1
IO_PSG
/IO_PSG
CLOCK
CLK
/CLK
U42
D1
D2
D3
D4
D5
D6
D7
D8
O1
O2
O3
O4
O5
O6
O7
O8
CLK
CLR
74LS273
U32
74LS1
U32
74LS0
U32
74LS0
U43A
74LS3
U43B
74LS3
U7C
74LS0
U44
7407
/WAIT
WAIT

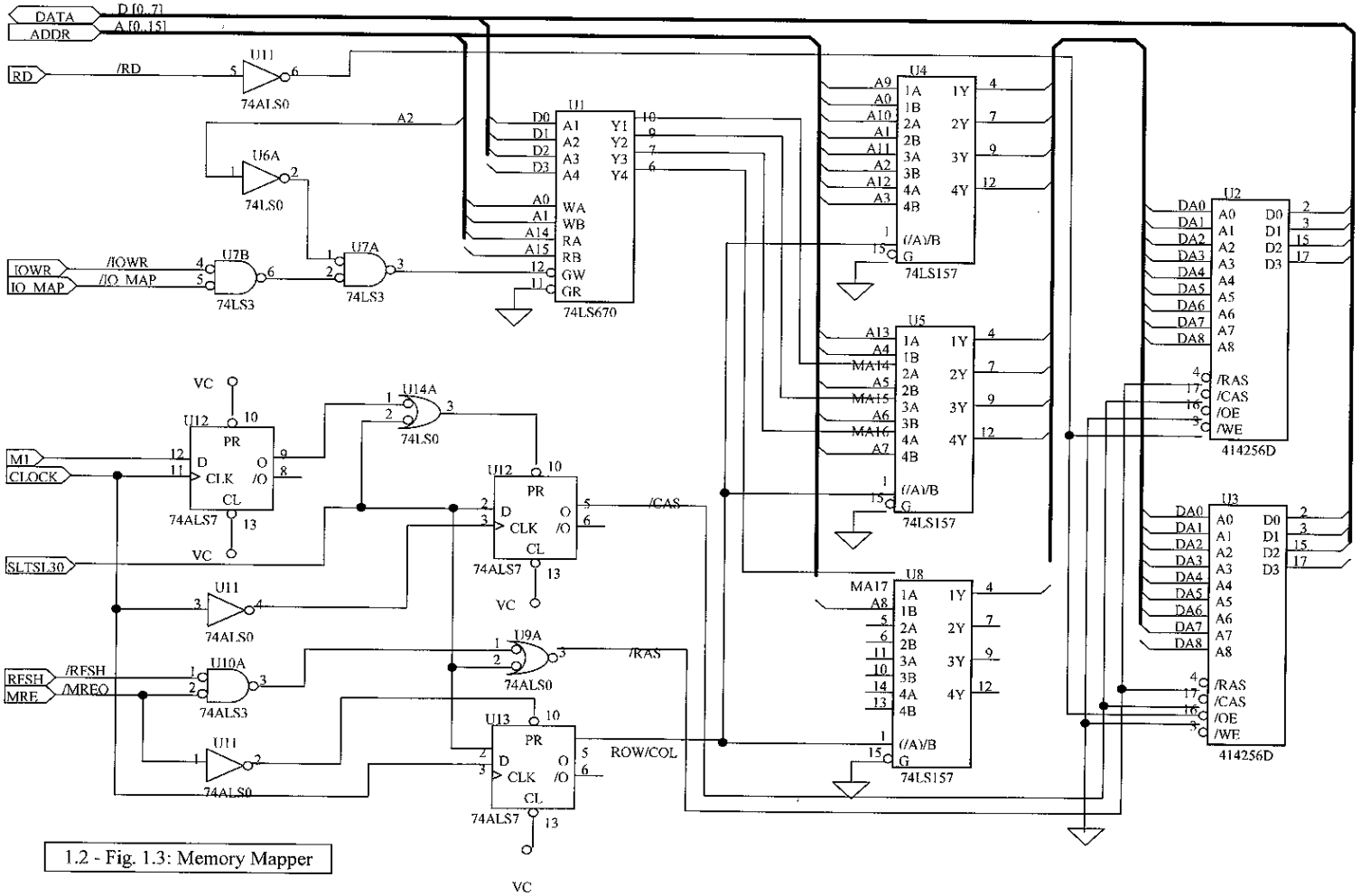


1.7.8 - Kanji ROM


DATA
D[0..7]
ADDR
A[0..15]
IO_PRN
/IO PRN
IOWR
/IOWR
IORD
/IORD
VCC
R11
R
U60
74LS138
/PRN CONT
/PRN DATA
U57B
74LS3
U55D
74LS3
U57A
74LS3
U56
74LS374
PR_D0
PR_D1
PR_D2
PR_D3
PR_D4
PR_D5
PR_D6
PR_D7
U59
RM
R9
R10
CN1
14 PIN
U41
74LS7
/PRN STB
U58
74LS125
/PRN RDY


DATA
D [0..7]
ADDR
A [0..15]
U62
74LS171
U19B
74LS13
U57D
74LS3
U57C
74LS3
U63A
74LS3
IO_RTC
RTC_EN
/IO_RTC
/RTC_EN
IORD
IOWR
/IORD
/IOWR
VC
C4
CAP
R13
R
X2
CRYSTA
C5
CAPACITOR
U61
RP5C01
OSCIN
OSCOU
/ALARM
ADJ
/CS
CS
/RD
/WR
U65
RM
R6 R5 R4 R3 R2 R1 C
U64
RM
C R1 R2 R3 R4 R5 R6 R7 R8
R12
300
VCC
Q2
PNP
Q1
NPN
C6
CAP
BT1
BATTERY
Q3
PNP
D1
R1
R2
R
1.7.10 - Real Time Clock


CLOCK
RD
MRE
RFSH
CS2
74LS365
U67
CS1
CS12
M1
IORO
WR
RESET
WAIT
INT
ADDR
DATA
A [0..15]
D [0..7]
U68
74LS245
U70
74LS540
U69
74LS540
U71A
74LS21
U63C
74LS3
U63B
74LS3
SLTSL1
SLTSL2
JP3
JP4
HEADER 25x2
SUNDIN2
SUNDIN1
VC
+5V
+12V
-12V
CARTRIDGE
CHECK CIRCUIT



1.2 - Fig. 1.3: Memory Mapper