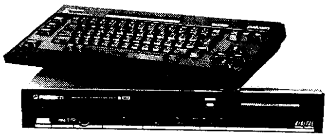
PIONEER

Service Manual

CIRCUIT & MECHANISM DESCRIPTIONS
REPAIR & ADJUSTMENTS



ORDER NO.
ARP-683-0

PERSONAL COMPUTER MSX

PX-7

MODEL PX-7 COMES IN TWO VERSIONS DISTINGUISHED AS FOLLOWS:

Type	Voltage	Remarks	RF OUTPUT
HE	AC220V, 240V (switchable)	European continent model	G/PAL UHF 36 ± 1 ch
HB	AC240V, 220V (switchable)	United Kingdom model	I/PAL UHF 36 ± 1 ch

- This service manual is applicable to the HE and HB types.

CONTENTS

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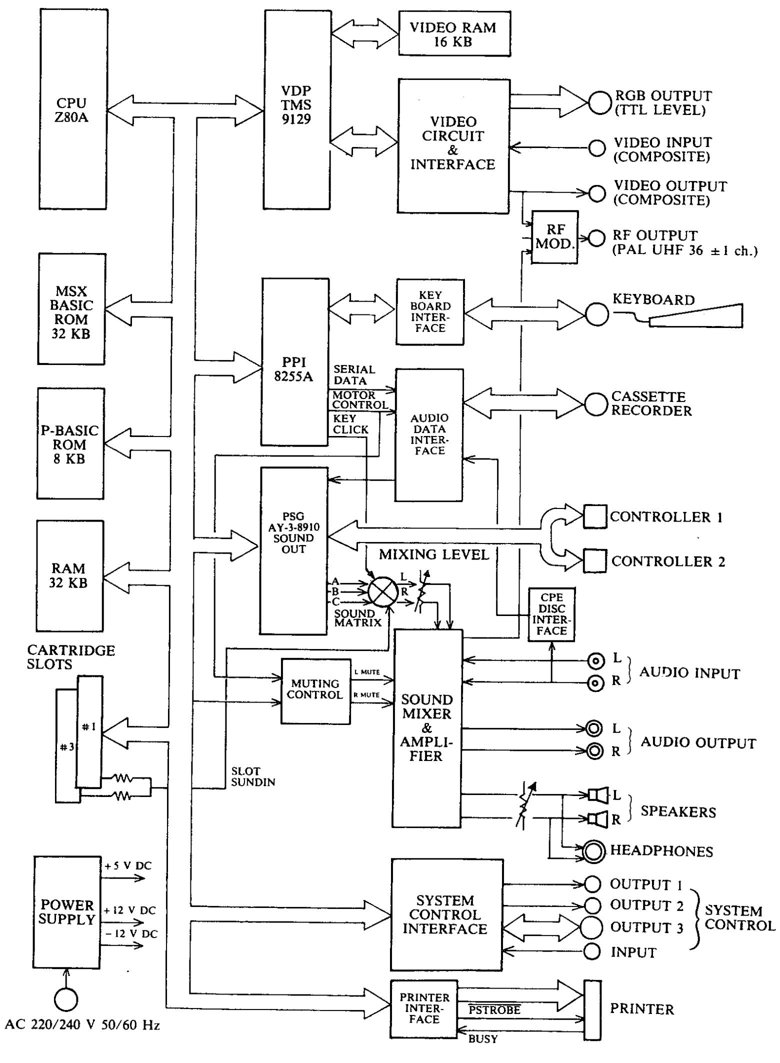
1.SPECIFICATIONS

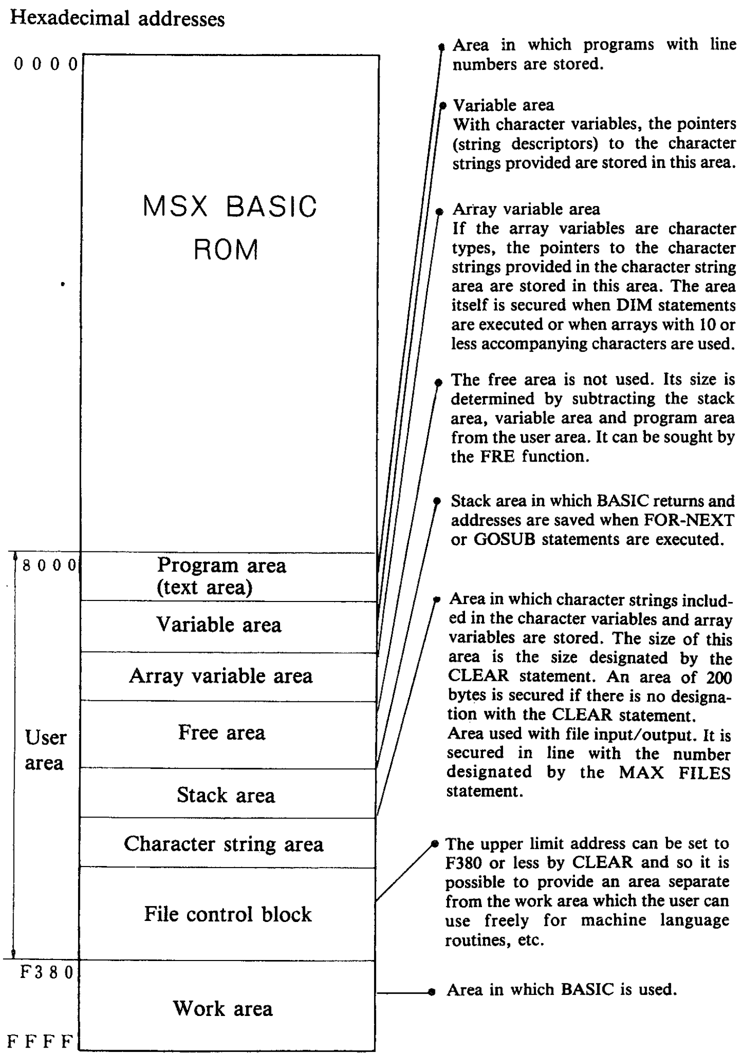
1. 1

CPU		8-bit Z80A (3.58 MHz clock)
Memory	RAM	48K (including 16K video RAM)
	ROM	40K (32K MSX BASIC, 8K P-BASIC)
Display	Text	SCREEN 0: 40 × 24 (default 37 × 24) SCREEN 1: 32 × 24 (default 29 × 24)
	Graphics resolution	256 × 192 dots
	Colors	16 colors
	Sprites	256 sprites
	Output	PAL composite video output (16 colours) 1Vp-p/75 Ω RGB output (8 colors), TTL level HB model: I/PAL/RF output (16 colors with sound) HE model: G/PAL/RF output (16 colors with sound) UHF 36 ±1 ch, 74 dBμV/75 Ω
	Screen control	Computer mode Superimpose mode External video mode
Keyboard	Type	Separate type, full stroke, 76 keys Cylindrical step sculptured key tops
	Facilities	Alphanumeric: 48 keys Control: 20 keys (with 4 cursor keys) Function: 5 keys (10 functions selectable) Screen mode control: 3 keys
	Cable	1.5 m with 13-pin DIN plug
Sound	Source	3 voice (8 octaves + 1 noise, 8 envelopes) 1 voice (key click sound) } Computer sound External stereo audio input signals 150 mV/50 kΩ
	Output	Internal speakers (stereo) Headphones (stereo) Line output (stereo), 150 mV/1 kΩ
	Mixing control	Computer sound mixing level control ±15 dB Master volume control External sound muting control
Interface	System control	Laser Vision Player, component display, audio system remote control ports
	Cassette recorder	Baud rate: 1200/2400 baud (software select) FSK signal
	Printer	Centronics standard, 8-bit parallel port
	Controller	Ports for 2 joysticks, tablets, paddles, trackballs, etc.
	Cartridge	2 MSX cartridge slots (slots #1 and #3)
Power requirements		220/240 V ±10%, 50/60 Hz, Power consumption: 37 W
Operating temperature		5—35 deg.C
Dimensions		Main unit: 420 (W)×323.5 (D)×70 (H) mm Keyboard: 420 (W)×171 (D)×47.5 (H) mm
Accessories		•Warranty card •RF cable (2 m) •Instruction manual •BASIC reference manual •P-BASIC reference manual

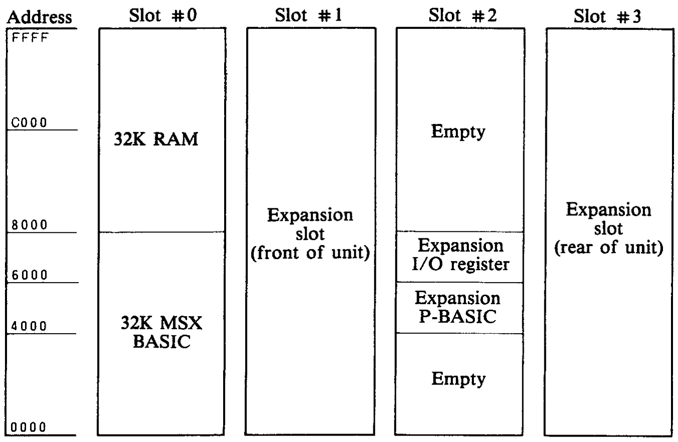
1. 2 BLOCK DIAGRAM



1. 3 MEMORY MAP

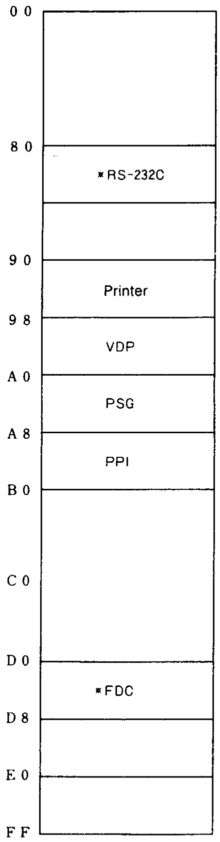


- **PX-7 Memory Configuration**



1. 4 I/O MAP

(1) I/O address allocation



	RW	Details	Remarks
&H98	W	Data write into VRAM	TMS9129NL or equivalent
	R	Data read from VRAM	
&H99	W	Command, address set	
	R	Status read	
&HA0	W	Address latch	AY-3-8910 or equivalent
&HA1	W	Data write	
&HA2	R	Data read	
&HA8	W	Port A data write	8255A or equivalent
	R	Port A data read	
&HA9	W	Port B data write	
	R	Port B data read	
&HAA	W	Port C data write	
	R	Port C data read	
&HAB	W	Mode set	
&H90	W	Strobe output (b0)	latch output
·	R	Status input (b1)	"1" is BUSY
&H91	W	Print data	latch output

I/O addresses from 80 to FF area prescribed as above for system use. Empty columns are system reserves.

*I/O addresses marked with an asterisk are for optional equipment.

(2) PPI bit allocation

Port	Bit	Input/ output	Signal	Details
A	0	Output	CS0L	Slot designation number of addresses
	1		CS0H	0000 to 3FFF
	2		CS1L	Slot designation number of addresses
	3		CS1H	4000 to 7FFF
	4		CS2L	Slot designation number of addresses
	5		CS2H	8000 to BFFF
	6		CS3L	Slot designation number of addresses
	7		CS3H	C000 to FFFF
B	0 ∫ 7	Input		Keyboard return signal
C	0	Output	KB0	Keyboard scan signals
	1		KB1	
	2		KB2	
	3		KB3	
	4		CASON	Cassette control (L-ON)
	5		CASW	Cassette write signal
	6		CAPS	CAPS lamp signal (lights when low)
	7		SOUND	Sound output based on software

(3) PSG bit allocation

Port	Bit	Input/ output	Connector pin no.	Signal when joystick used
A	0	Input	CONTROLLER 1-1 pin *1	FWD1
			CONTROLLER 2-1 pin *2	FWD2
	1		CONTROLLER 1-2 pin *1	BACK1
			CONTROLLER 2-2 pin *2	BACK2
	2		CONTROLLER 1-3 pin *1	LEFT1
			CONTROLLER 2-3 pin *2	LEFT2
	3		CONTROLLER 1-4 pin *1	RIGHT1
			CONTROLLER 2-4 pin *2	RIGHT2
	4		CONTROLLER 1-6 pin *1	TRGA1
			CONTROLLER 2-6 pin *2	TRGA2
	5		CONTROLLER 1-7 pin *1	TRGB1
			CONTROLLER 2-7 pin *2	TRGB2
	6			
	7		CASR (cassette tape read)	
B	0	Output	CONTROLLER 1-6 pin *3	High level
	1		CONTROLLER 1-7 pin *3	High level
	2		CONTROLLER 2-6 pin *3	High level
	3		CONTROLLER 2-7 pin *3	High level
	4		CONTROLLER 1-8 —	
	5		CONTROLLER 2-8 —	
	6		Port A input select	
	7			

*1: Effective when port B bit 6 is low. For CONTROLLER 1
*2: Effective when port B bit 6 is high. For CONTROLLER 2
*3: Set high when the port is not used as an output port.

(4) Expansion I/O registers (slot #2)

LCON register <7FFE (16)>

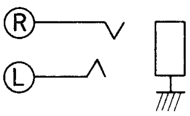
Bit	RW	Signal	Function
7	R	$\overline{\text{ACK}}$	Significant with acknowledge 1→0 with respect to remote control signal transmission
6			Not used
1			Not used
0	R	RMCLOK	Clock produced by dividing CLK1/CLK2 frequency by 128
	W	$\overline{\text{REM}}$	High output with bit serial data output generated in synchronization with RMCLK

VCON register <7FFF (16)>

Bit	RW	Signal	Function
7	R	$\overline{\text{EXTV}}$	Status indicating availability of external video signal. Low when available; high when not available.
	W	Mute	Line input signal muting
6			Not used
1			Not used
0	R	INTEXV	Interrupt available with interrupt flag 1 when external video signal is OFF. Set to 0 when read.
	W	$\overline{\text{OVERLAY}}$	Hardware selection signal of superimpose/non-superimpose mode; 0 for superimpose, 1 for non-superimpose

1. 5 CONNECTOR

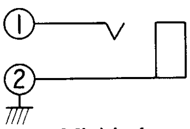
(1) System control output 1



R $\overline{\text{VOVLY}}$ (OUT)
L $\overline{\text{EXTREMO}}$(OUT)

Stereo mini-jack

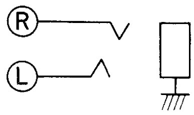
(3) System control output 2



① CREMO(OUT)
② GND

Mini-jack

(2) System control input

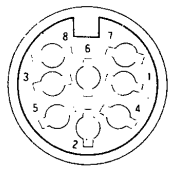


R $\overline{\text{SELECT I}}$(IN)
L $\overline{\text{EXTREM I}}$(IN)

Stereo mini-jack

(4) System control output 3

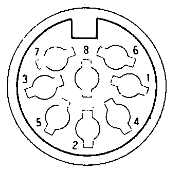
Pin No.	Signal	I/O
1	$\overline{SELECTO}$	O
2	-	-
3	-	-
4	$\overline{LACK}$	I
5	-	-
6	-	-
7	$\overline{LREMO}$	O
8	-	-



Horseshoe-shaped
8-pin DIN connector

(5) RGB connector

Pin No.	Signal	Logical porality
1	-	-
2	GND	-
3	-	-
4	Horizontal sync signal	Negative
5	Vertical sync signal	Negative
6	RED	Positive
7	GREEN	Positive
8	BLUE	Positive

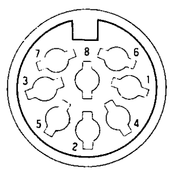


Round 8-pin DIN connector

(6) Cassette interface connector

Pin No.	Signal	I/O*
1	GND	-
2	GND	-
3	GND	-
4	CMT OUT	0
5	CMT IN	I
6	REM+	0
7	REM–	0
8	GND	-

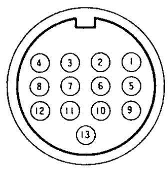
*INPUT or OUTPUT based on unit.



Round 8-pin DIN connector

(7) Keyboard interface connector

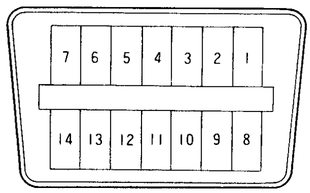
Pin No.	Signal	I/O
1	D6	I
2	D5	I
3	D2	I/O
4	D1	I/O
5	D7	I
6	D3	I
7	D4	I/O
8	D0	I/O
9	+5 V	-
10	STB	O
11	GND	-
12	$\overline{\text{CAPS}}$	O
13	GND	-



Round 13-pin connector

(8) Printer connector

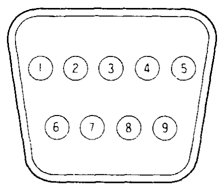
Pin No.	Signal	I/O
1	$\overline{\text{PSTB}}$	O
2	PDB0	O
3	PDB1	O
4	PDB2	O
5	PDB3	O
6	PDB4	O
7	PDB5	O
8	PDB6	O
9	PDB7	O
10	NC	-
11	BUSY	I
12	NC	-
13	NC	-
14	GND	-



Amphenol 14-pin connector

(9) Controller connector

Pin No.	Signal	I/O
1	$\overline{\text{FWD}}$	I
2	$\overline{\text{BACK}}$	I
3	$\overline{\text{LEFT}}$	I
4	$\overline{\text{RIGHT}}$	I
5	+5 V	-
6	$\overline{\text{TRG1}}$	I/O
7	$\overline{\text{TRG2}}$	I/O
8	OUTPUT	O
9	GND	-

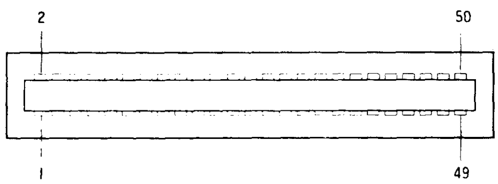


DSUB type 9-pin connector

(10) Cartridge connector

Pin No.	Signal	I/O*	Pin No.	Signal	I/O*
1	$\overline{\text{CS1}}$	O	2	$\overline{\text{CS2}}$	O
3	$\overline{\text{CS12}}$	O	4	$\overline{\text{SLTSL}}$	O
5	Spare	-	6	$\overline{\text{RFSH}}$	O
7	$\overline{\text{WAIT}}$	I	8	$\overline{\text{INT}}$	I
9	$\overline{\text{M1}}$	O	10	$\overline{\text{BUSDIR}}$	I
11	$\overline{\text{IORQ}}$	O	12	$\overline{\text{MERQ}}$	O
13	$\overline{\text{WR}}$	O	14	$\overline{\text{RD}}$	O
15	$\overline{\text{RESET}}$	O	16	Spare	-
17	A9	O	18	A15	O
19	A11	O	20	A10	O
21	A7	O	22	A6	O
23	A12	O	24	A8	O
25	A14	O	26	A13	O
27	A1	O	28	A0	O
29	A3	O	30	A2	O
31	A5	O	32	A4	O
33	D1	I/O	34	D0	I/O
35	D3	I/O	36	D2	I/O
37	D5	I/O	38	D4	I/O
39	D7	I/O	40	D6	I/O
41	GND	-	42	CLOCK	O
43	GND	-	44	SW1	-
45	+5 V	-	46	SW2	-
47	+5 V	-	48	+12 V	-
49	SUNDIN	I	50	−12 V	-

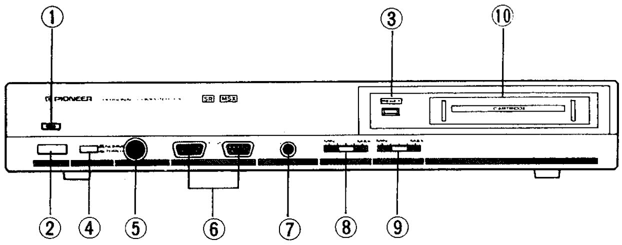
*Input or output based on unit.



Note: The spare pins are not to be used.

2. PANEL FACILITIES

(1) FRONT PANEL FACILITIES



① POWER indicator

This lights up red when power is supplied to the PX-7.

② POWER switch

Power is supplied to the PX-7 when this switch is pressed and the POWER indicator lights. Press the switch again to turn off the power.

③ RESET switch

When this switch is pressed, the computer is reset and set to the same state as when the power is turned on.

④ VIDEO • AUDIO switch

This is used to select the output signals of the rear panel output terminals (VIDEO/ AUDIO) or of the built-in speakers.

- ■ NORMAL: The signals that pass through the PX-7's circuitry are output to the rear panel output terminals. The picture on the connected display is selected by operating the screen selector key on the keyboard.
- ▬ THROUGH: The signals which were input to the rear panel input terminals are output, without being passed through the PX-7's circuitry, to the rear panel output terminals. The sound supplied from the PX-7 is heard through the built-in speakers.

⑤ KEYBOARD connector

The keyboard cable is connected here. Make sure that the cutout on the connector is facing up and insert securely.

⑥ CONTROLLER connectors (1, 2)

Connect a joystick or tablet to these connectors. When two units are connected, the left-hand connector is treated as No. 1 and the right-hand connector as No. 2.

⑦ PHONES jack

Connect the headphones to this jack. The sound from the built-in speakers is no longer heard when the headphone plug is connected to this jack.

⑧ VOLUME control

Use this control to adjust the volume of the built-in speakers or headphones. The volume is increased when the control is slid from MIN toward the MAX setting.

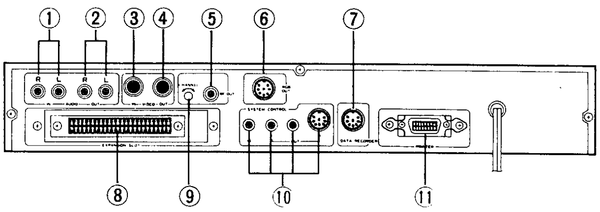
⑨ MIXING LEVEL control

This adjusts the mixing level of the sound generated by the PX-7 and the external audio signals connected to the rear panel AUDIO INPUT terminals. The sound generated by the PX-7 is increased when the control is slid from the MIN toward the MAX setting.

⑩ CARTRIDGE slot

Insert a game or other cartridge into this slot.

(2) REAR PANEL FACILITIES



① AUDIO INPUT terminals (R, L)

Connect the external audio signals (such as the audio output of the video disc player) to these terminals.

② AUDIO OUTPUT terminals (R, L)

Use these terminals to connect an external stereo amplifier. They are used when the sound of the personal computer is to be passed through the stereo circuitry.

③ VIDEO INPUT terminal

Connect the external video signal (such as the video output of the video disc player) to this terminal.

④ VIDEO OUTPUT terminal

This is connected to the video input terminal on a display unit.

⑤ RF OUTPUT connector

This is used when a TV set without a video input terminal is to be employed as the display unit. Use the accessory RF cable to connect this terminal with the antenna input terminal on the TV set.

⑥ RGB OUTPUT connector

This is used when connection is made to a display unit equipped with an RGB input connector.

⑦ DATA RECORDER connector

Connect a tape recorder to this connector.

⑧ EXPANSION SLOT

A game cartridge or other cartridge, such as an MSX floppy disc drive cartridge, is plugged in here.

⑨ CHANNEL ADJUSTMENT knob

By turning this knob with a small flat-bladed screwdriver, adjustments can be made for ±1 channel

↺ : +1 ch (37 ch)
↻ : −1 ch (35 ch)

⑩ SYSTEM CONTROL terminals

INPUT:	This is the input terminal of the control signal. Use it when the unit is employed in combination with PIONEER's SD-26 component display unit.
OUTPUT 1:	The control signals from the PX-7 are output here. Use it when the unit is employed in combination with PIONEER's SD-R5 RGB system control pack.
OUTPUT 2:	The control signals from the PX-7 are output here. Use it when the unit is employed in combination with PIONEER's LD-1100 Laser vision player.
OUTPUT 3:	The control signals from the PX-7 are output here. Use it when the unit is employed in combination with PIONEER's LD-700 Laser vision player.

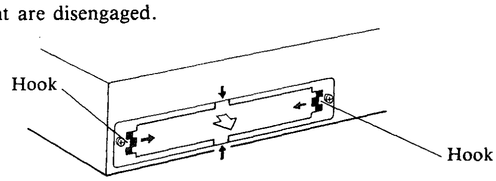
Note:
See pages 18 through 21 when using the unit in combination with PIONEER's SD-26 component display or with the LD-1100 or LD-700 Laser vision player.

⑪ PRINTER connector

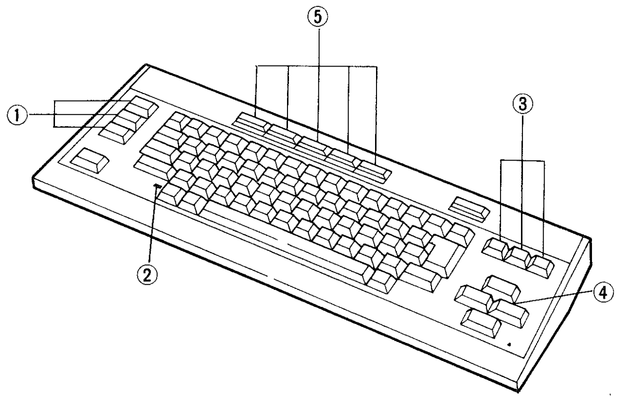
Connect the printer here.

• Removing the expansion slot cover

A cover is provided over the expansion slot on the rear panel of the computer for shipment. Remove it, as shown in the figure, when using this slot. It can be removed when the center part is pulled toward you and the hooks on the left and right are disengaged.



(3) KEYBOARD



① Screen selector keys

These are used to select the screen on the display connected to the PX-7.

SUPERIMPOSE:	The superimposed picture, resulting from the PX-7's picture and the picture of the external video source which has been connected to the video input terminal on the PX-7's rear panel, appears on the display.
VIDEO:	The picture of the external video source which has been connected to the PX-7's video input terminal appears on the display.
COMPUTER:	The computer picture generated by the PX-7 appears on the display.

② Upper case indicator

This lights when the CAPS LOCK key is pressed to enter upper-case letters.

③ Screen editing keys (CLS HOME, INS, DEL)

These keys are used to edit the letters displayed on the screen.

④ Cursor keys

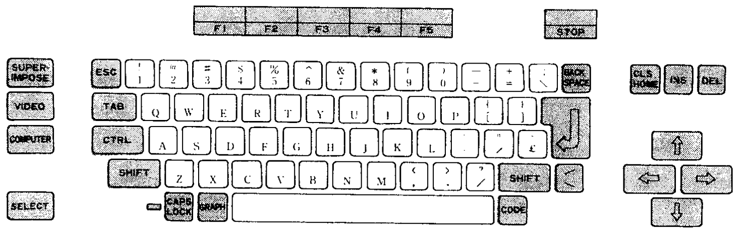
These are used to move the cursor vertically and horizontally.

⑤ Function keys

When one of these keys is pressed, the character string defined by that key is entered.

(4) KEY FUNCTIONS

The unit's keyboard layout is shown below.



Keys indicated by ▧ in the figure are called special keys and are differentiated from the other (character) keys. A description of the special keys is given first.

● Special Keys

SHIFT This key is used to type upper-case English letters, and characters indicated on the top part of the other character keys. A SHIFT key is provided both on the left and right sides of the keyboard; either key may be used.

CAPS LOCK This is used to type upper-case of the character which has lower-case and uppercase. It is locked when pressed once and the lamp to the left of the key top lights. It is released when pressed again. When character keys are pressed with this key locked, upper-case are typed and when the key is released, lowercase are typed.

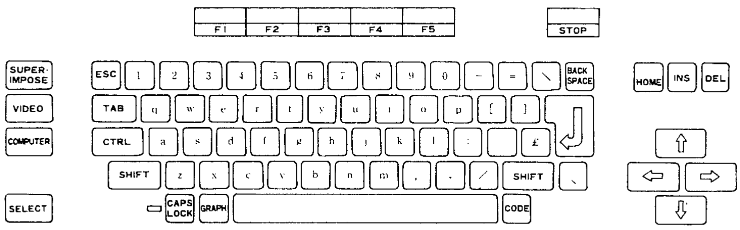
GRAPH This is used to type graphic characters. When a character key is pressed when this key is pressed or when this key and the SHIFT key are simultaneously pressed, graphic characters are typed.

CODE This is used to type special characters. When a character key is pressed when this key is pressed or when this key and the SHIFT key are simultaneously pressed, special characters are typed.

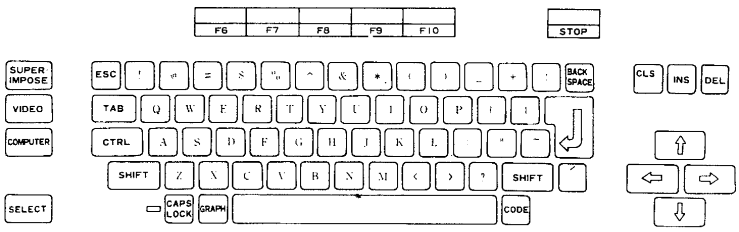
● Character symbols displayed on the screen

When the alphanumeric keys are pressed, the character symbols entered on the screen change depending on whether the [SHIFT], [GRAPH] or [CODE] keys, or a combination of those keys, are used, See below for more details.

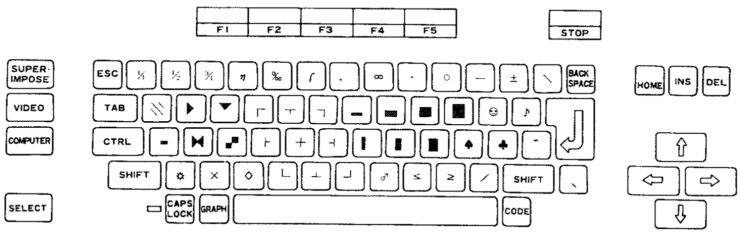
(a) When the alphanumeric keys alone are pressed:



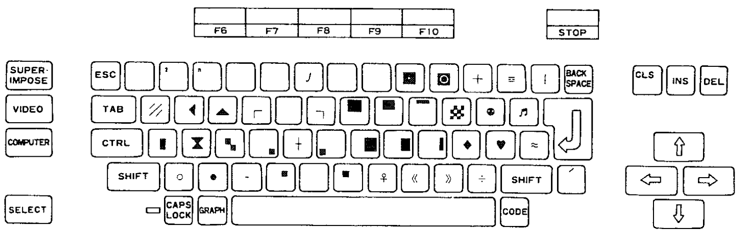
(b) When the alphanumeric keys are pressed while the [SHIFT] key is depressed:



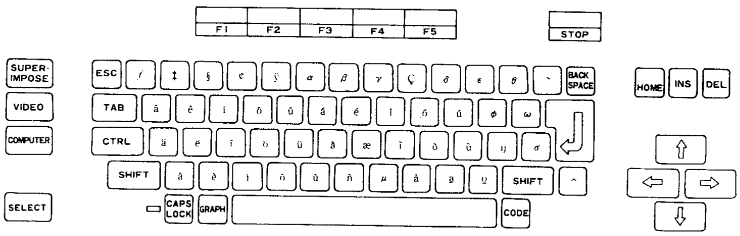
(c) When the alphanumeric keys are pressed while the [GRAPH] key is depressed:



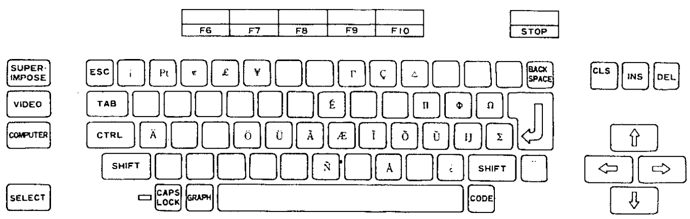
(d) When the alphanumeric keys are pressed while the [GRAPH] and [SHIFT] keys are depressed:



(e) When the alphanumeric keys are pressed while the [CODE] key is depressed:



(f) When the alphanumeric keys are pressed while the [CODE] and [SHIFT] keys are depressed:

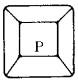


> *Note:*
> - *SCREEN MODE 0 is for text only. Part of the graphic character font may disappear. Use SCREEN MODE 1 when operating the alphanumeric keys together with the [GRAPH] key.*

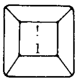
● Character Keys

Several characters can be typed with a single character key. The character to be typed can be selected in combination with the special keys.
"+" and "," signify the following:

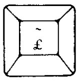
[A] + [B]	Press the [B] key with the [A] key depressed.
[A] ,	Press the [A] key once and keep in the [A] key mode.



Key pressed	Typed character
[P]	p (Lower case)
[SHIFT] + [P]	P (Upper case)
[CAPS] , [P]	P (Upper case)
[CAPS] , [SHIFT] + [P]	P (Upper case)
[GRAPH] + [P]	■ (Graphic symbol mode)
[GRAPH] + [SHIFT] + [P]	▚ (Graphic symbol mode)
[CODE] + [P]	ú (Special character mode)
[CODE] + [SHIFT] + [P]	Π (Special character mode)



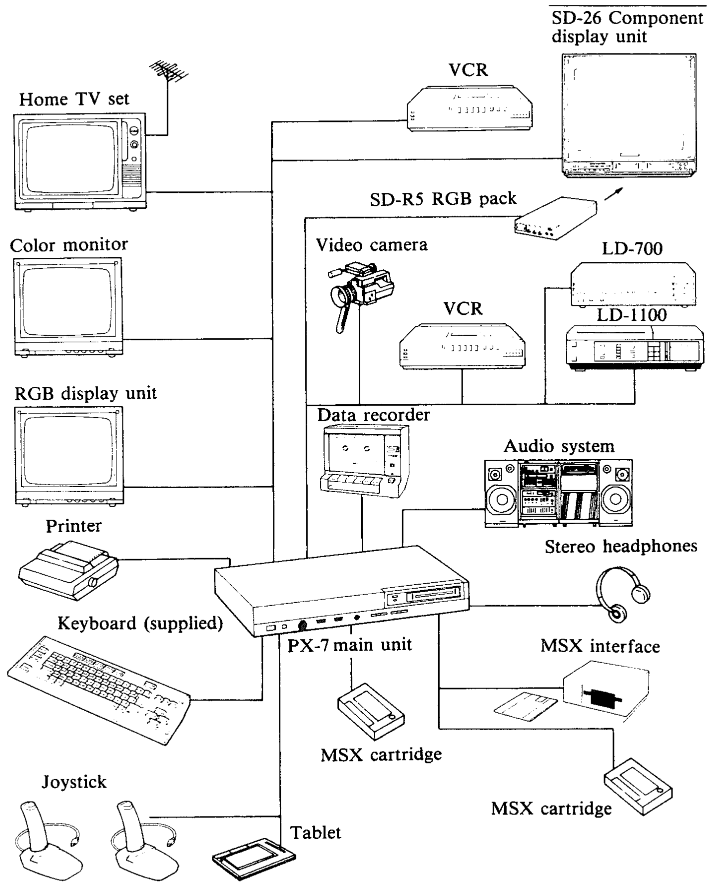
Key pressed	Typed character
[!/1]	1
[SHIFT] + [!/1]	!
[CAPS] , [!/1]	1
[CAPS] , [SHIFT] + [!/1]	!
[GRAPH] + [!/1]	¼
[CODE] + [!/1]	f
[CODE] + [SHIFT] + [!/1]	¡



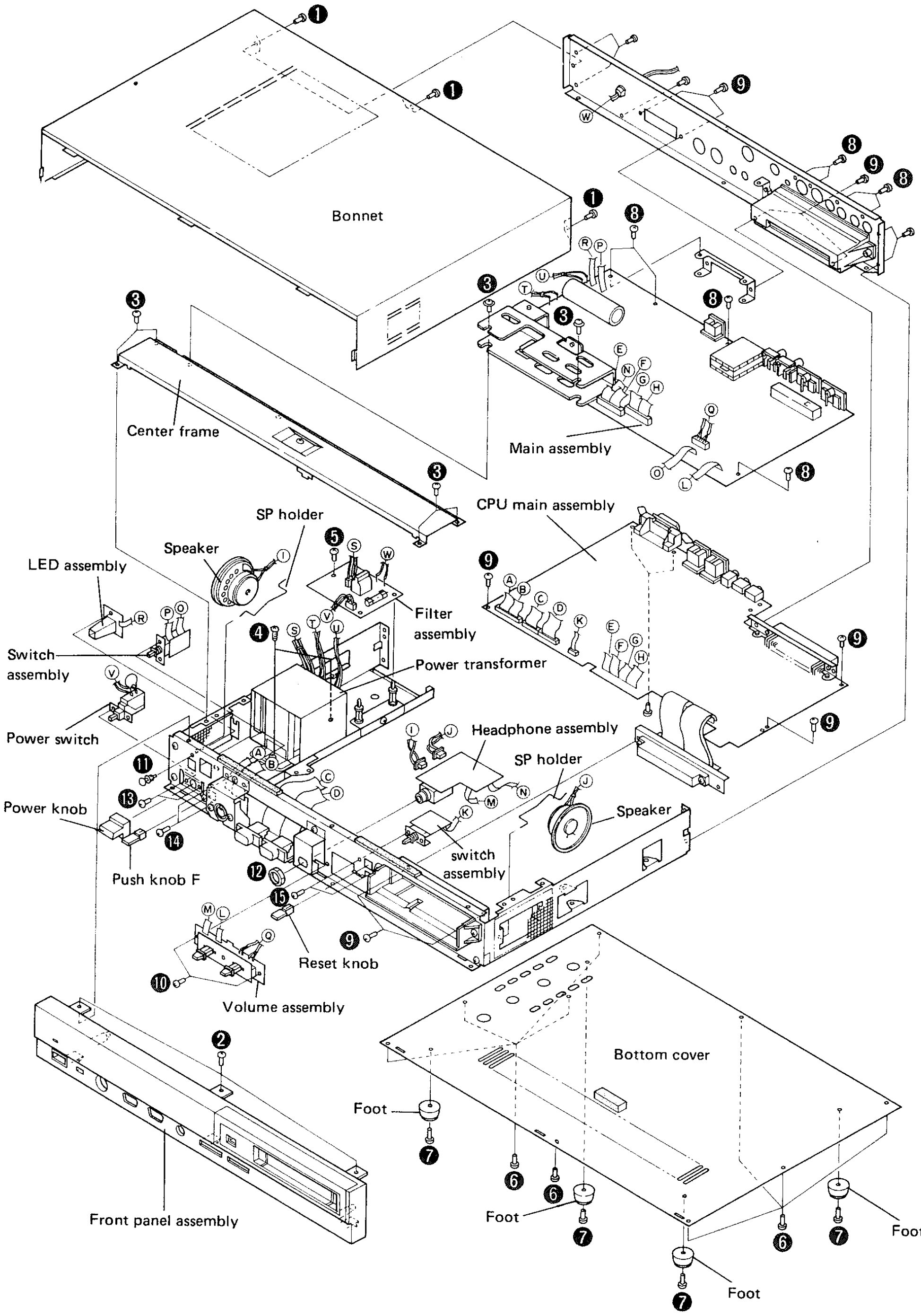
Key pressed	Typed character
[~/£]	£
[SHIFT] + [~/£]	~
[GRAPH] + [~/£]	‿
[GRAPH] + [SHIFT] + [~/£]	≈
[CODE] + [~/£]	σ
[CODE] + [SHIFT] + [~/£]	Σ

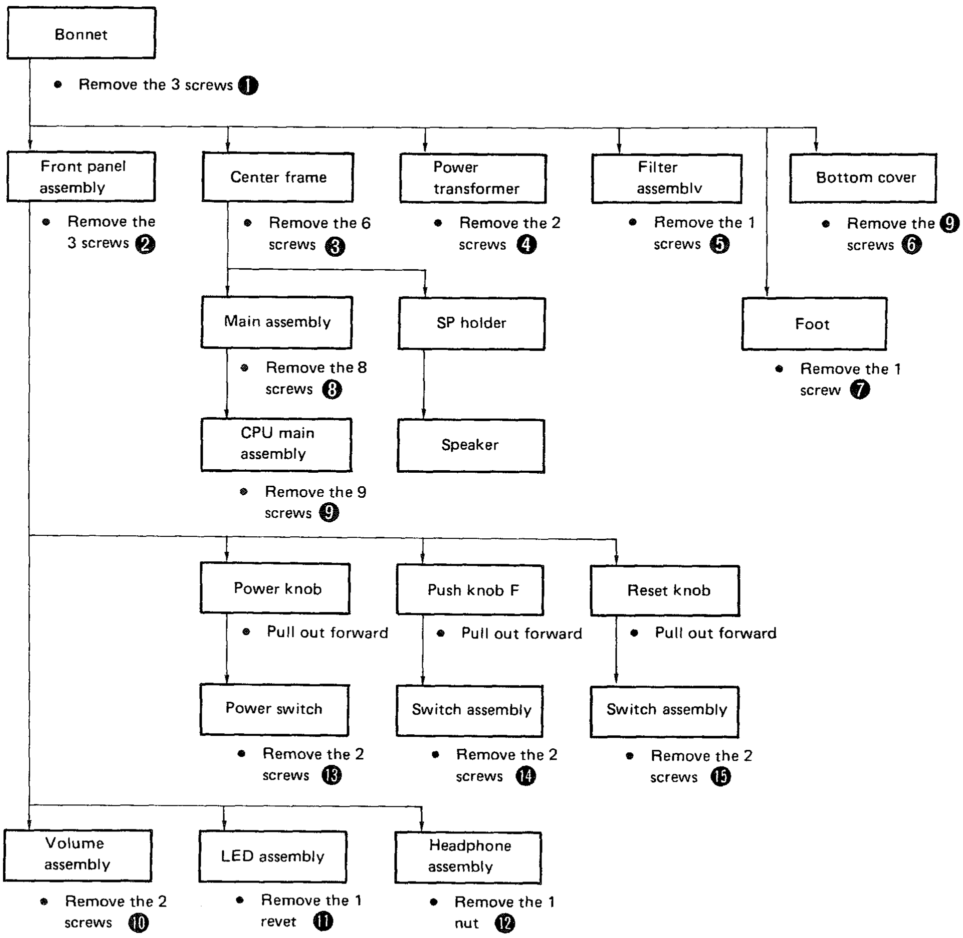
• SYSTEM CONFIGURATION

The PX-7 not only opens the door to system expansion with MSX-standard peripheral units but also makes the most of its features through couplıng with a video disc player. If a VCR and an audio system are further added, systems completely unavailable in the past can be built up. The system configuration of the PX-7 is shown in the figure below.



3.DISASSEMBLY



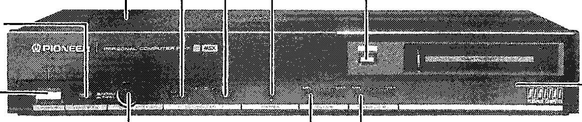


Bonnet
• Remove the 3 screws ❶
Front panel assembly
• Remove the 3 screws ❷
Center frame
• Remove the 6 screws ❸
Power transformer
• Remove the 2 screws ❹
Filter assemblv
• Remove the 1 screws ❺
Bottom cover
• Remove the ❾ screws ❻
Main assembly
• Remove the 8 screws ❽
SP holder
Foot
• Remove the 1 screw ❼
CPU main assembly
• Remove the 9 screws ❾
Speaker
Power knob
• Pull out forward
Push knob F
• Pull out forward
Reset knob
• Pull out forward
Power switch
• Remove the 2 screws ⓭
Switch assembly
• Remove the 2 screws ⓮
Switch assembly
• Remove the 2 screws ⓯
Volume assembly
• Remove the 2 screws ❿
LED assembly
• Remove the 1 revet ⓫
Headphone assembly
• Remove the 1 nut ⓬

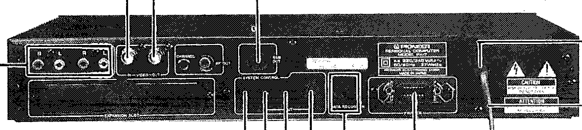
4. PARTS LOCATIONS

NOTES:
- *The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.*
- *For your Parts Stock Control, the fast moving items are indicated with the marks ★★ and ★.*
  ★★ GENERALLY MOVES FASTER THAN ★
  This classification shall be adjusted by each distributor because it depends on model number, temperature, humidity, etc.

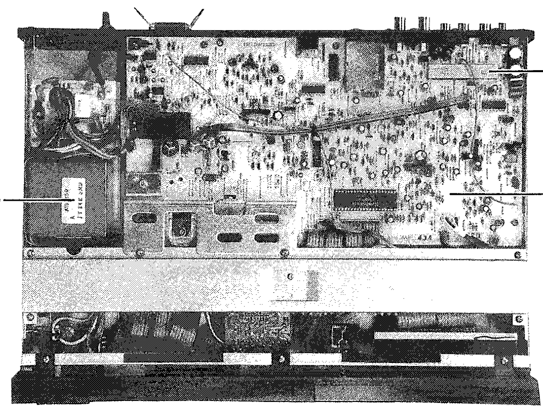
Front Panel View



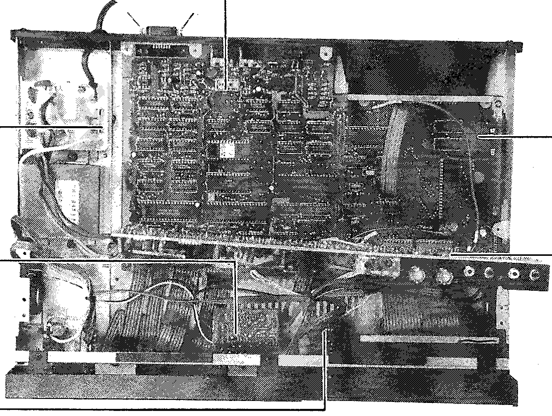
Rear Panel View



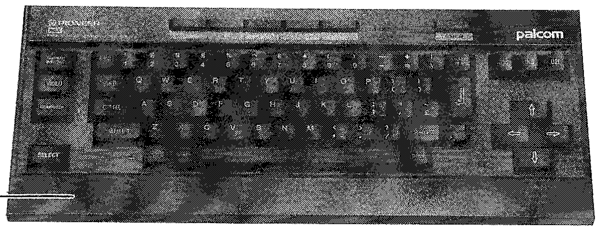
Top View I



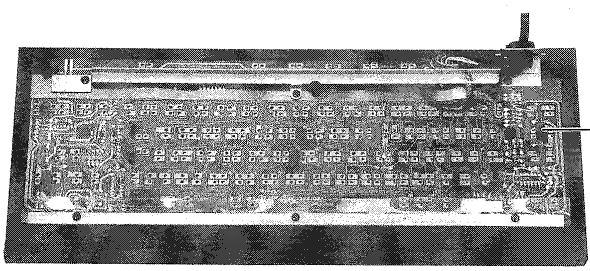
Top View II



KEY BOARD ASSEMBLY

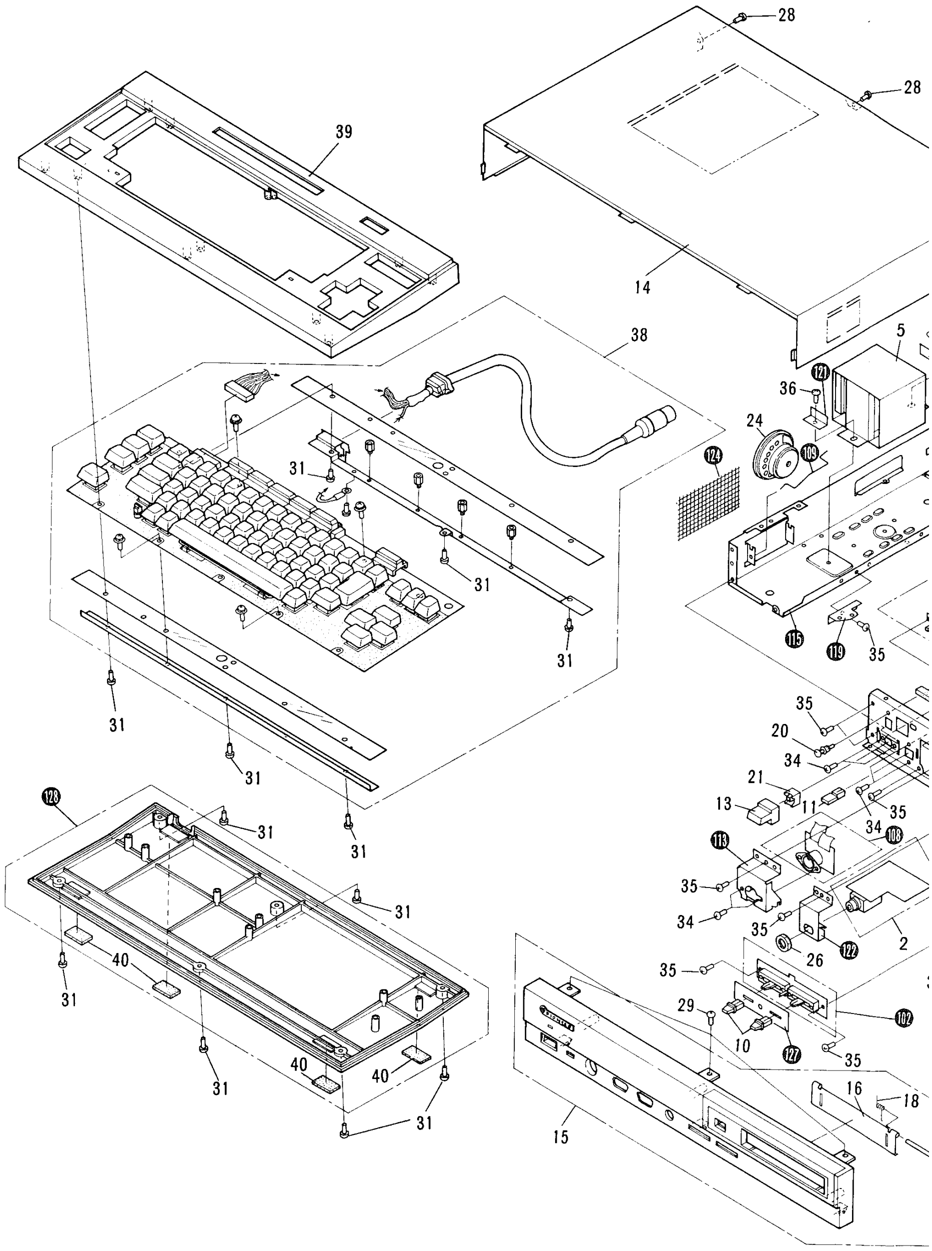


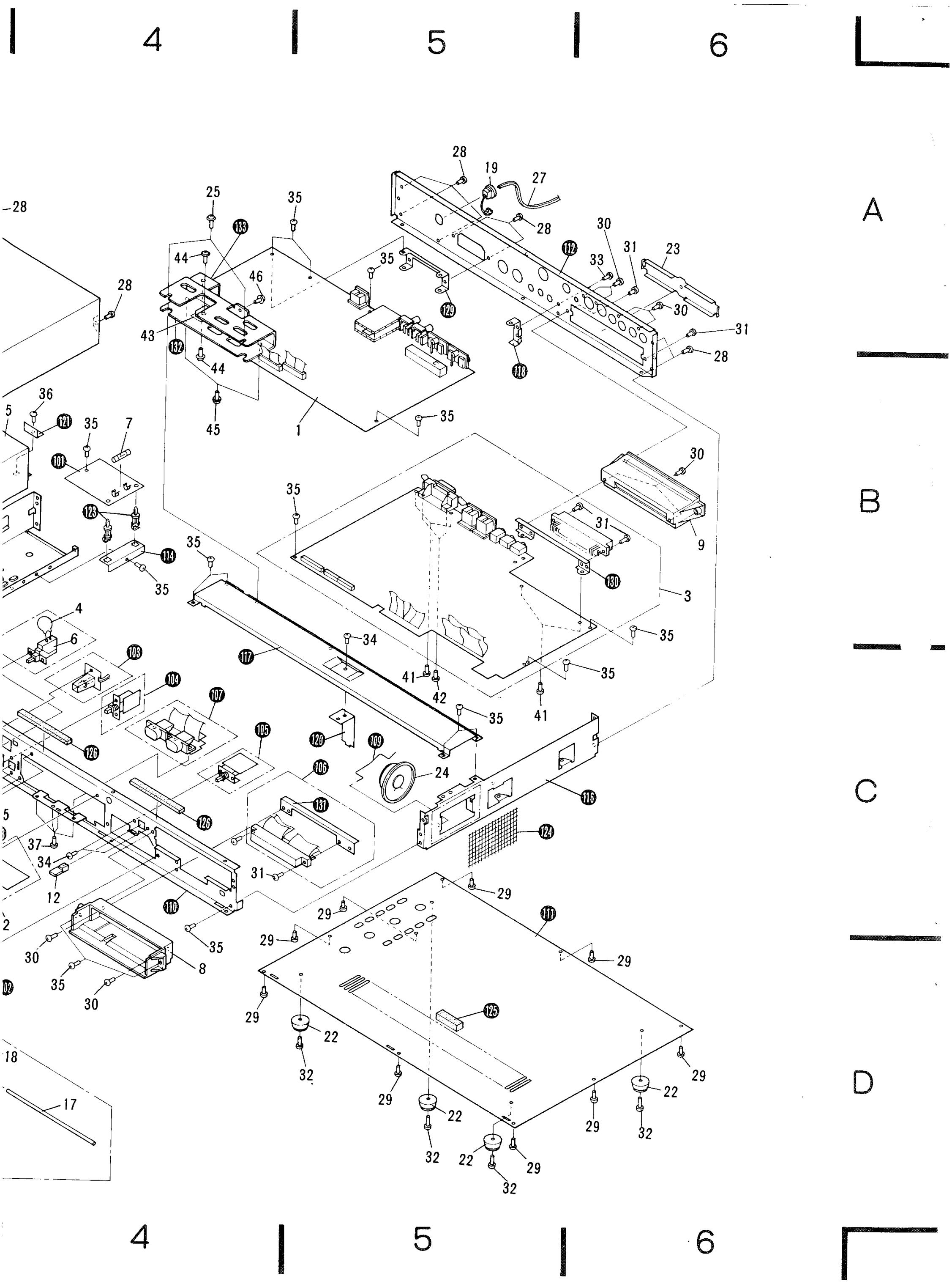
Bottom View



5.EXPLODED VIEWS AND PARTS LIST

A
B
C
D



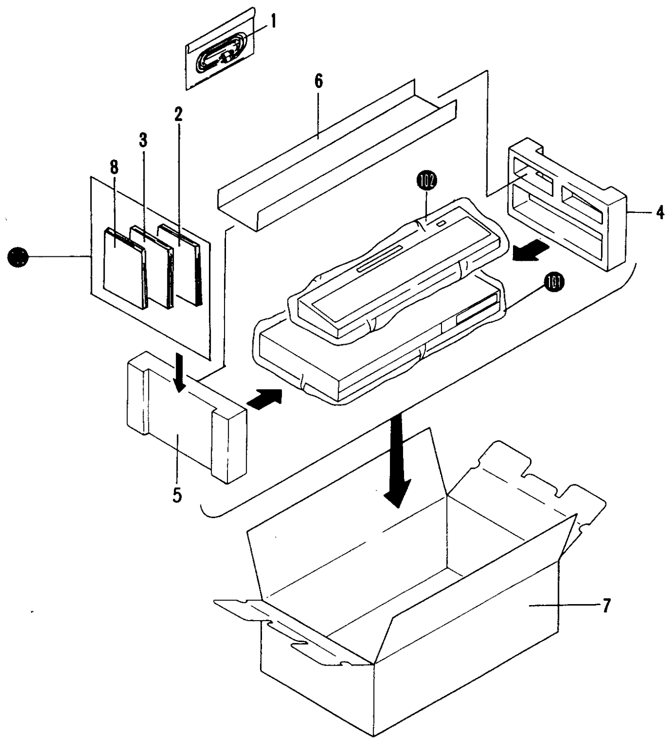

4
5
6
A
B
C
D
4
5
6

NOTES:
- ***Parts without part number cannot be supplied.***
- ***The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.***
- ***For your Parts Stock Control, the fast moving items are indicated with the marks ★★ and ★.***
  ★★ GENERALLY MOVES FASTER THAN ★
  This classification shall be adjusted by each distributor because it depends on model number, temperature, humidity, etc.

Parts List of Exploded View

Mark	No.	Part No.	Description
	1.	GWM-419 (HB)	Main assembly
		GWM-434 (HE)	
	2.	GWH-184	Push switch (S2: POWER)
	3.	GWP-141	CPU main assembly
	4.	ACG-504	Capacitor (C80)
⚠ ★	5.	ATS-250	Power transformer (T1: 240V)
⚠ ★★	6.	ASG-539	Push switch (S2 POWER)
⚠ ★★	7.	AEK-502	Fuse (FU101: T200mA/250V)
	8.	ANZ-157	Cartridge holder (F)
	9.	ANZ-158	Cartridge holder (R)
	10.	AAD-892	Slide knob (VOLUME/MIXING)
	11.	AAY-294	Push knob F (VIDEO • AUDIO)
	12.	AAY-295	Reset knob (RESET)
	13.	AAY-296	Power knob (POWER)
	14.	ANE-591	Bonnet
	15.	ANY-101	Front panel assembly
	16.	AAH-111	Cartridge door
	17.	ANL-034	Door Shaft
	18.	ABH-158	Door Spring
⚠	19.	AEC-327	Strain relief
	20.	AEC-441	Plastic rivet
	21.	AEC-800	Flexible ring
	22.	AEP-306	Leg
	23.	AEP-308	Slot cover
★★	24.	APV-008	Speaker
	25.	ABA-252	Screw 3 x 8
	26.	ABN-065	Nut
⚠	27.	ADG-051 (HB)	AC power cord
		ADG-041 (HE)	
	28.	BBT30P080FZK	Screw 3 x 8
	29.	BBZ30P050FMC	Screw 3 x 5
	30.	BBZ30P080FZK	Screw 3 x 8
	31.	BBZ30P100FZK	Screw 3 x 10
	32.	BCZ30P080FMC	Screw 3 x 8
	33.	BMZ30P080FZB	Screw 3 x 8
	34.	PMZ30P060FMC	Screw 3 x 6
	35.	VBZ30P080FMC	Screw 3 x 8
	36.	VBZ40P060FMC	Screw 4 x 6
	37.	VPZ30P080FMC	Screw 3 x 8
	38.	AWX-324	Key board assembly
	39.	ANY-103	Front cover assembly
	40.	AEB-287	Foot
	41.	VBZ30P080FZK	Screw 3 x 8
	42.	BBZ40P080FZK	Screw 4 x 8
	43.	AEP-056	Sheet
	44.	ABA-234	Screw
	45.	ABA-284	Screw
	46.	PBZ30P060FMC	Screw 3 x 6
	101.		Filter assembly
	102.		Volume assembly
	103.		LED assembly
	104.		Switch assembly
	105.		Switch assembly
	106.		Slot connector assembly
	107.		Joy stic connector assembly
	108.		Key board connector assembly
	109.		SP holder
	110.		Front chassis
	111.		Bottom cover
	112.		Rear panel
	113.		CN bracket
	114.		P.C. B. bracket
	115.		Side chassis (L)
	116.		Side chassis (R)
	117.		Center frame
	118.		P.C.B. bracket (1)
	119.		P.C.B. bracket (2)
	120.		P.C.B. bracket (3)
	121.		L angle
	122.		Jack bracket
	123.		P.C.B. holder
	124.		SP net
	125.		Cushion A
	126.		Cushion B
	127.		VR mask
	128.		Buttom case assembly
	129.		P.C.N. bracket
	130.		CN angle (2)
	131.		CN angle (1)
	132.		Heat sink
	133.		Heat sink

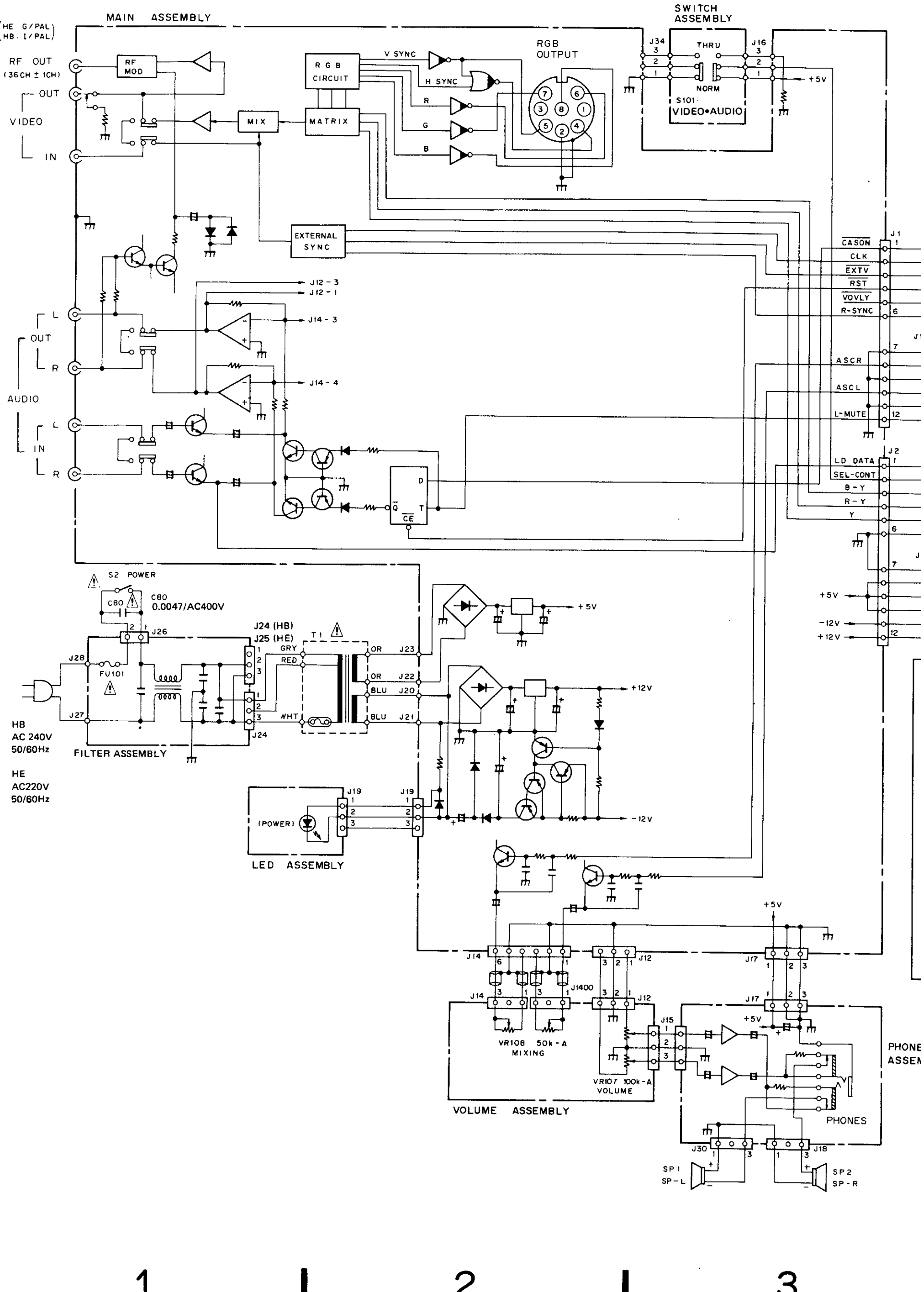
6.PACKING

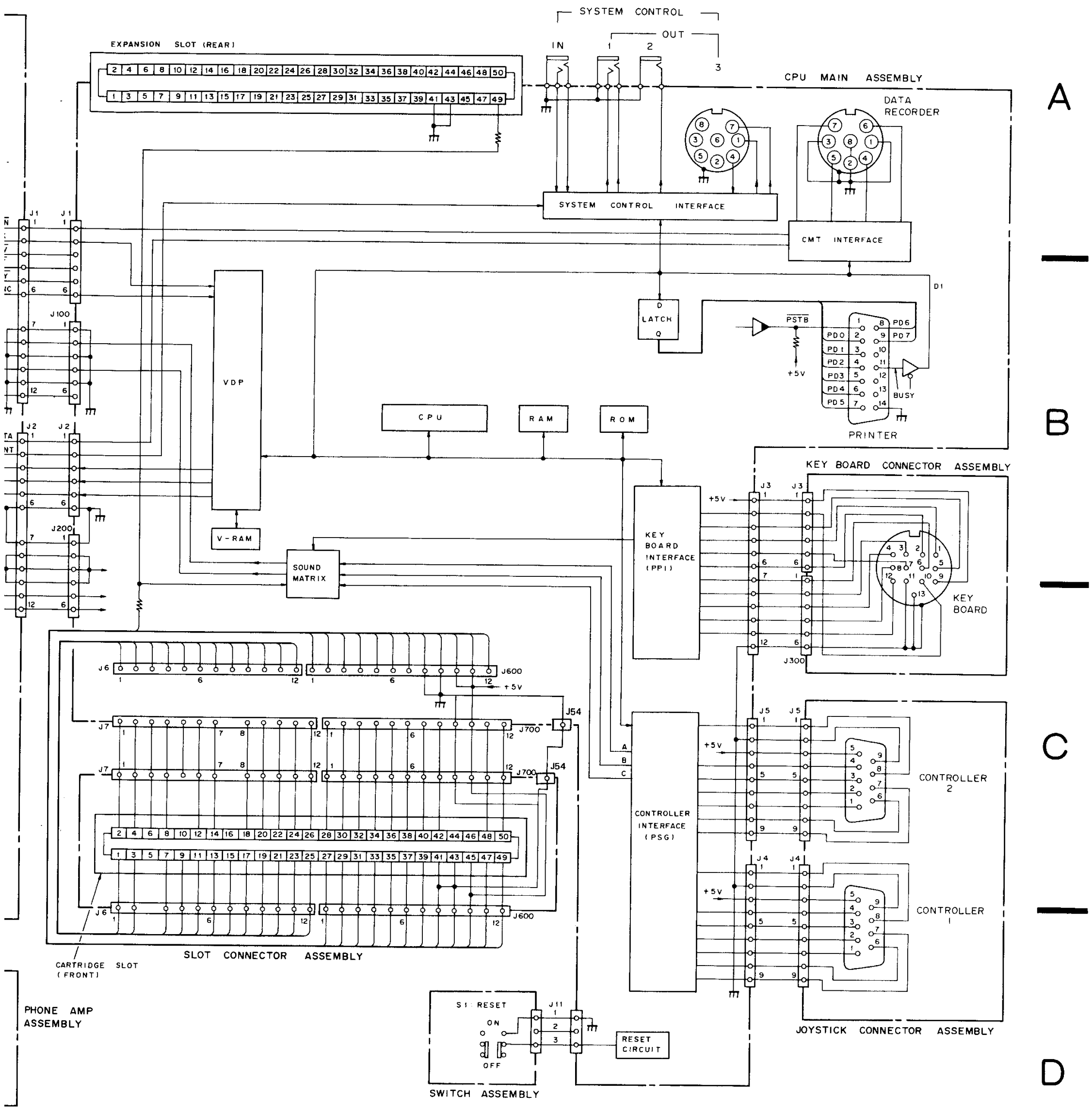


Parts List of Packing

Mark	No.	Part No.	Description	Mark	No.	Part No.	Description
	1.	ADE-094	Cord		6.	AHB-154	Spacer
	2.	ARB-697	Instruction manual		7.	AHE-625	Packing case
	3.	ARB-698	Basic manual		8.	ARB-703	P. Basic manual
	4.	AHA-405	Packing (A)				
	5.	AHA-406	Packing (B)		101.		Bag
					102.		Bag
					103.		Bag

7. CONNECTION DIAGRAM

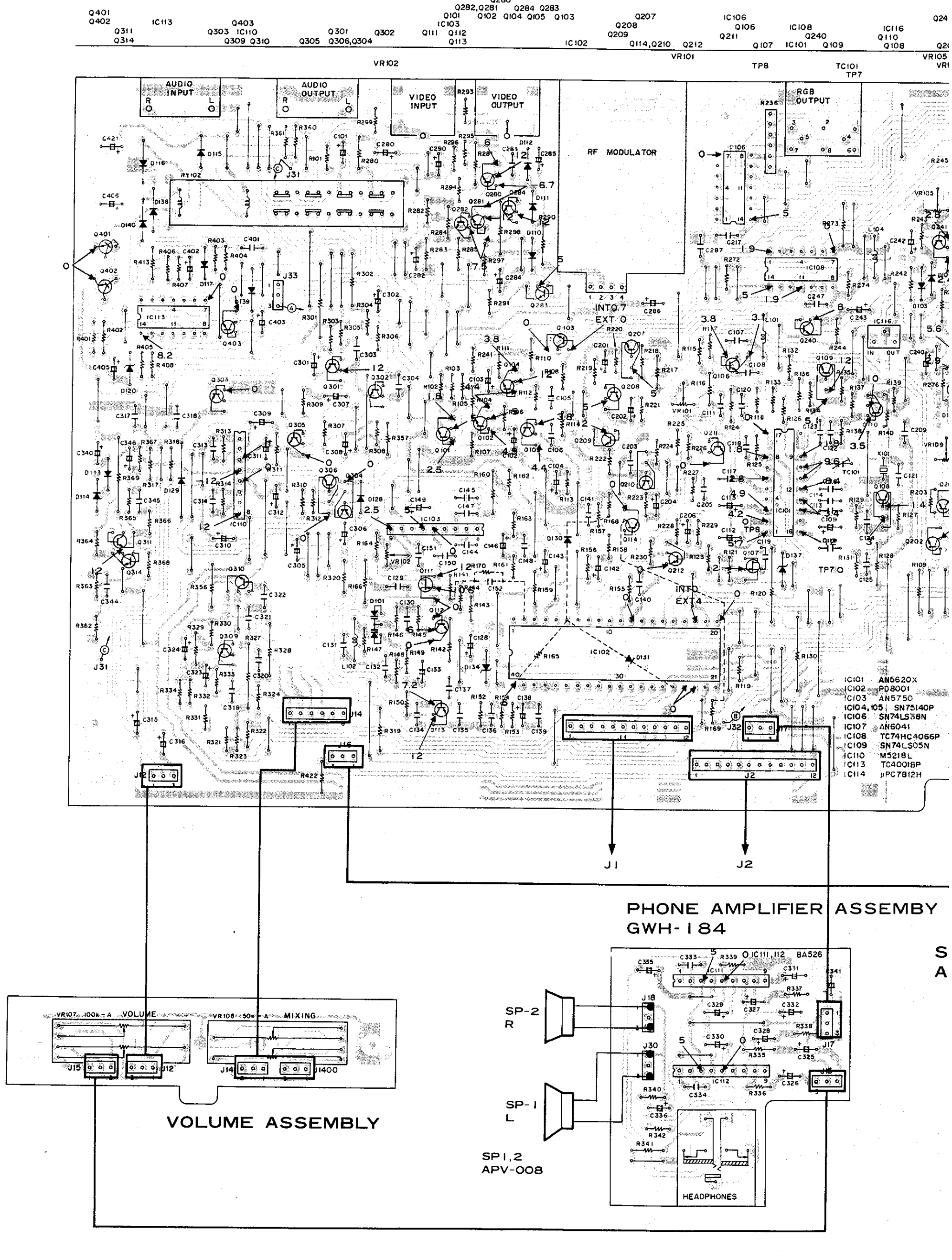



SYSTEM CONTROL
IN
OUT
1
2
3
EXPANSION SLOT (REAR)
CPU MAIN ASSEMBLY
DATA RECORDER
SYSTEM CONTROL INTERFACE
CMT INTERFACE
J1
J100
J2
J200
VDP
V-RAM
LATCH
PSTB
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
BUSY
+5V
PRINTER
CPU
RAM
ROM
KEY BOARD CONNECTOR ASSEMBLY
KEY BOARD INTERFACE (PPI)
J3
J300
KEY BOARD
SOUND MATRIX
J6
J600
J7
J700
J54
CONTROLLER INTERFACE (PSG)
J5
J4
CONTROLLER 2
CONTROLLER 1
JOYSTICK CONNECTOR ASSEMBLY
SLOT CONNECTOR ASSEMBLY
CARTRIDGE SLOT (FRONT)
PHONE AMP ASSEMBLY
S1 RESET
ON
OFF
J11
RESET CIRCUIT
SWITCH ASSEMBLY
A
B
C
D

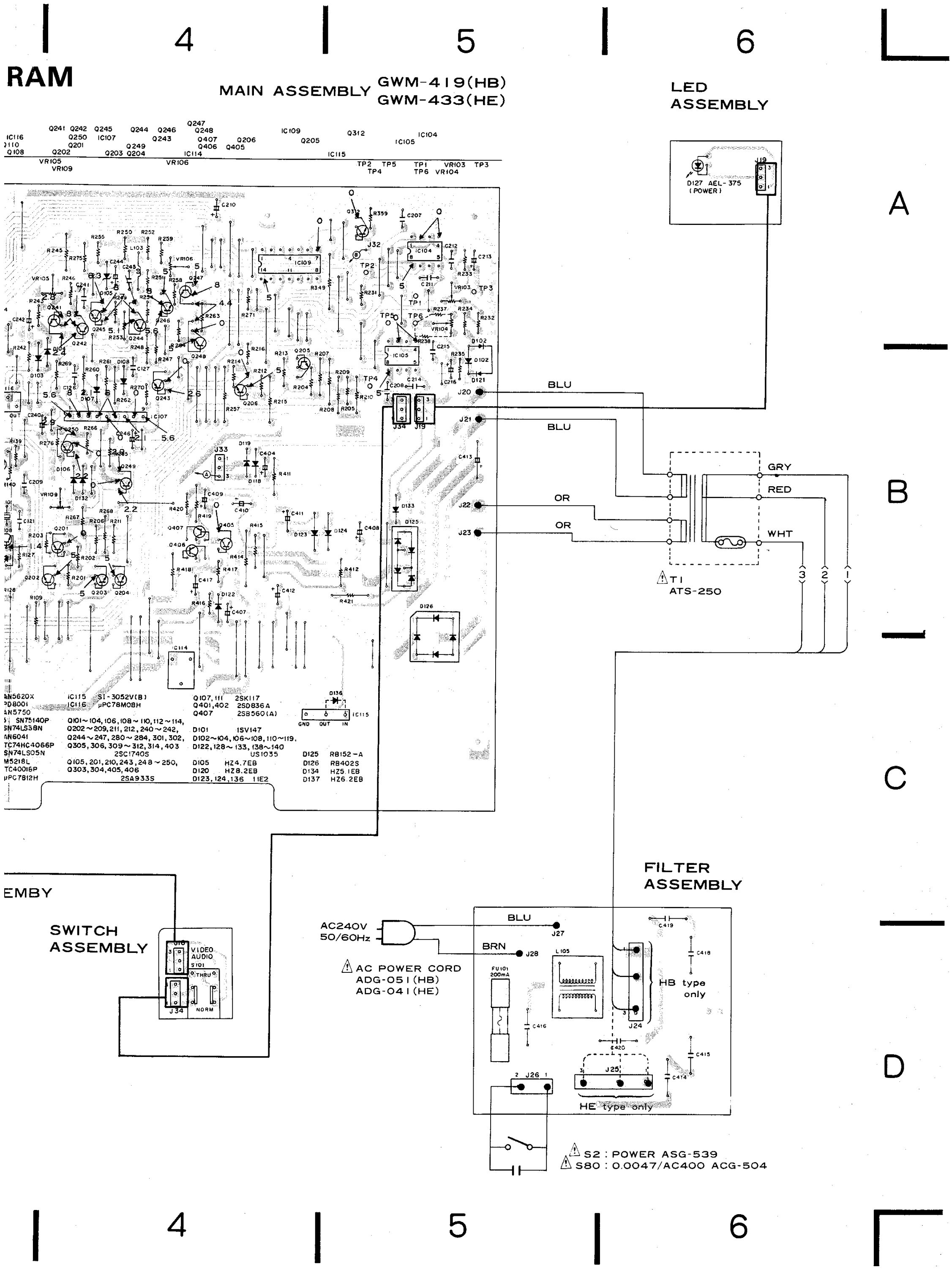
1 2 3

8.SCHEMATIC AND P,C,BOARDS CONNECTION DIAGRAM

8.1 MAIN ASSEMBLY



1 2 3


RAM
MAIN ASSEMBLY GWM-419(HB) GWM-433(HE)
LED ASSEMBLY
D127 AEL-375 (POWER)
BLU
BLU
GRY
RED
OR
OR
WHT
T1
ATS-250
EMBY
SWITCH ASSEMBLY
FILTER ASSEMBLY
AC240V 50/60Hz
BLU
BRN
AC POWER CORD
ADG-051(HB)
ADG-041(HE)
HB type only
HE type only
S2 : POWER ASG-539
S80 : 0.0047/AC400 ACG-504
4
5
6
A
B
C
D

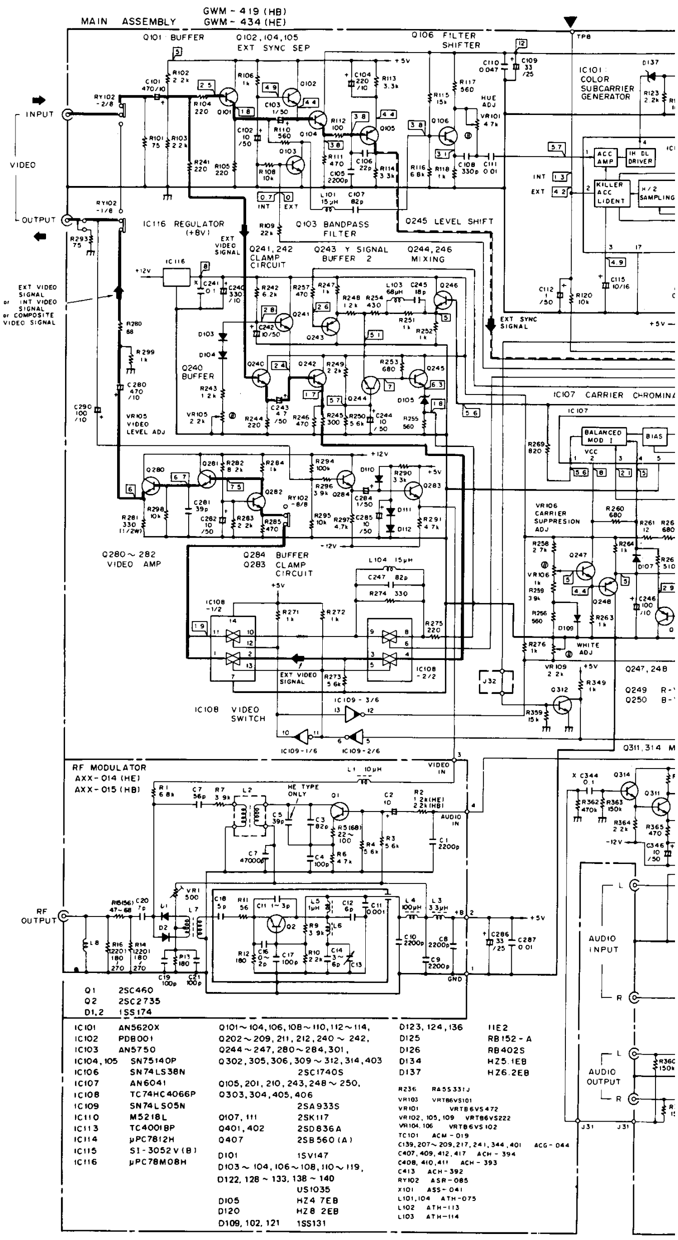
1 2 3

A

B

C

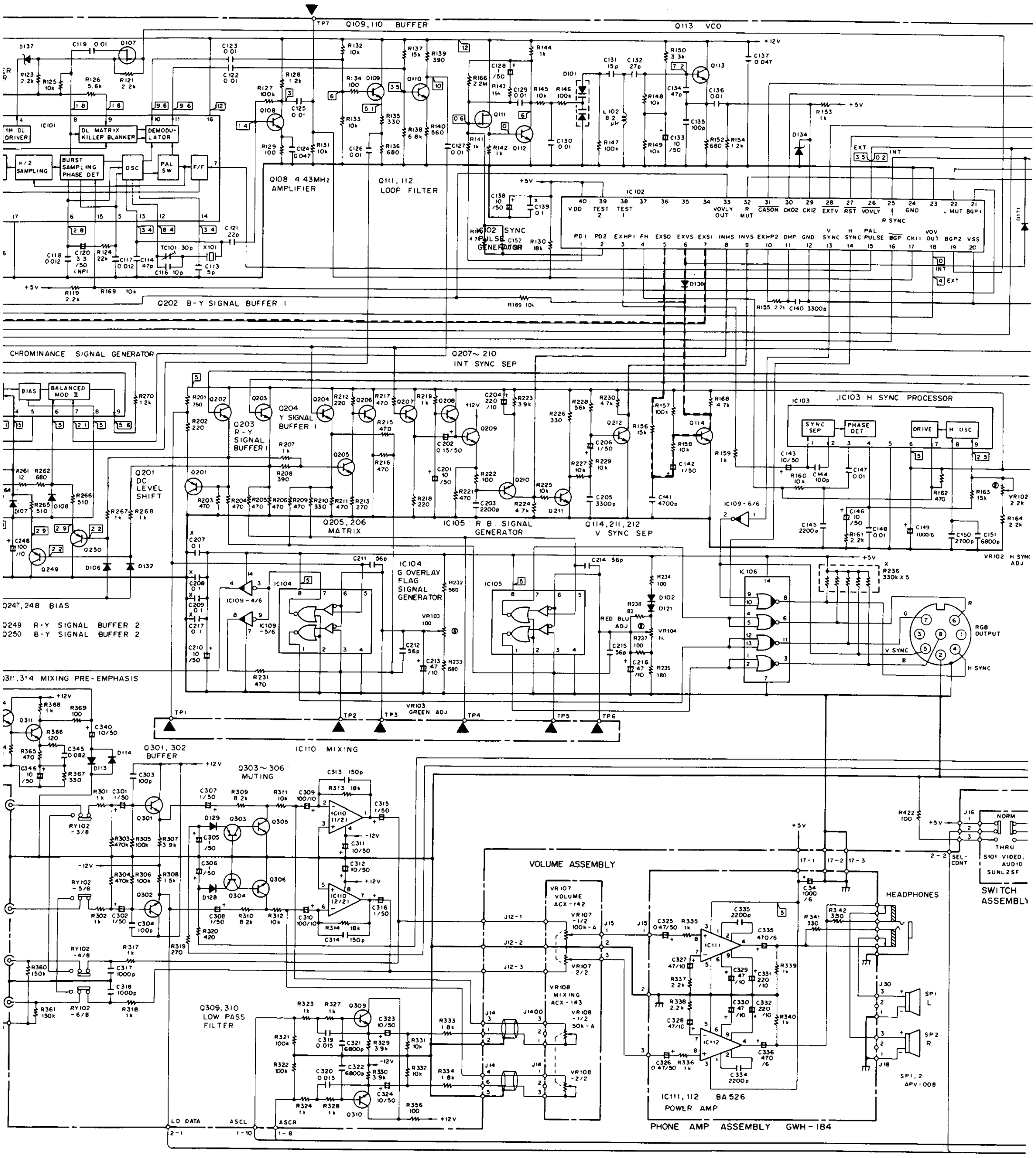
D



MAIN ASSEMBLY GWM-419 (HB) GWM-434 (HE)
Q101 BUFFER
Q102, 104, 105 EXT SYNC SEP
Q106 FILTER SHIFTER
IC101 COLOR SUBCARRIER GENERATOR
INPUT
VIDEO
OUTPUT
Q103 BANDPASS FILTER
Q245 LEVEL SHIFT
IC116 REGULATOR (+8V)
EXT VIDEO SIGNAL
Q241, 242 CLAMP CIRCUIT
Q243 Y SIGNAL BUFFER 2
Q244, 246 MIXING
EXT VIDEO SIGNAL or INT VIDEO SIGNAL or COMPOSITE VIDEO SIGNAL
EXT SYNC SIGNAL
Q240 BUFFER
VR105 VIDEO LEVEL ADJ
IC107 CARRIER CHROMINA
BALANCED MOD I
VR106 CARRIER SUPPRESION ADJ
WHITE ADJ
Q280 ~ 282 VIDEO AMP
Q284 BUFFER
Q283 CLAMP CIRCUIT
IC108 VIDEO SWITCH
Q247, 248
RF MODULATOR AXX-014 (HE) AXX-015 (HB)
HE TYPE ONLY
VIDEO IN
AUDIO IN
RF OUTPUT
GND
AUDIO INPUT
AUDIO OUTPUT
Q1 2SC460
Q2 2SC2735
D1, 2 1SS174
IC101 AN5620X
IC102 PDB001
IC103 AN5750
IC104, 105 SN75140P
IC106 SN74LS38N
IC107 AN6041
IC108 TC74HC4066P
IC109 SN74LS05N
IC110 M5218L
IC113 TC4001BP
IC114 μPC7812H
IC115 S1-3052V (B)
IC116 μPC78M08H
Q101 ~ 104, 106, 108 ~ 110, 112 ~ 114,
Q202 ~ 209, 211, 212, 240 ~ 242,
Q244 ~ 247, 280 ~ 284, 301,
Q302, 305, 306, 309 ~ 312, 314, 403 2SC1740S
Q105, 201, 210, 243, 248 ~ 250,
Q303, 304, 405, 406 2SA933S
Q107, 111 2SK117
Q401, 402 2SD836A
Q407 2SB560 (A)
D101 1SV147
D103 ~ 104, 106 ~ 108, 110 ~ 119,
D122, 128 ~ 133, 138 ~ 140 US1035
D105 HZ4 7EB
D120 HZ8 2EB
D109, 102, 121 1SS131
D123, 124, 136 11E2
D125 RB152-A
D126 RB402S
D134 HZ5 1EB
D137 HZ6.2EB

1 2 3

4 5 6



Q109, 110 BUFFER
Q113 VCO
Q108 4.43MHz AMPLIFIER
Q111, 112 LOOP FILTER
IC102
Q202 B-Y SIGNAL BUFFER 1
CHROMINANCE SIGNAL GENERATOR
Q207～210 INT SYNC SEP
IC103 H SYNC PROCESSOR
Q203 R-Y SIGNAL BUFFER 1
Q204 Y SIGNAL BUFFER 1
Q201 DC LEVEL SHIFT
Q205, 206 MATRIX
IC105 R B SIGNAL GENERATOR
Q114, 211, 212 V SYNC SEP
IC104 G OVERLAY FLAG SIGNAL GENERATOR
RGB OUTPUT
Q247, 248 BIAS
Q249 R-Y SIGNAL BUFFER 2
Q250 B-Y SIGNAL BUFFER 2
IC110 MIXING
Q301, 302 BUFFER
Q303～306 MUTING
VOLUME ASSEMBLY
HEADPHONES
SWITCH ASSEMBLY
Q309, 310 LOW PASS FILTER
IC111, 112 BA526 POWER AMP
PHONE AMP ASSEMBLY GWH-184

4 5 6

1. RESISTORS
Indicated in Ω, ¼W, ⅛W, ±5% tolerance unless otherwise noted k, kΩ, M, MΩ, (F), ±1%, (G), ±2%, (K), ±10%, (M), ±20% tolerance

2. CAPACITORS
Indicated in capacity (μF)/voltage (V) unless otherwise noted p, pF. Indication without voltage is 50V except electrolytic capacitor.

3. VOLTAGE CURRENT.
▭ ; DC voltage (V) at no input signal
Value in ( ) is DC voltage at rated power

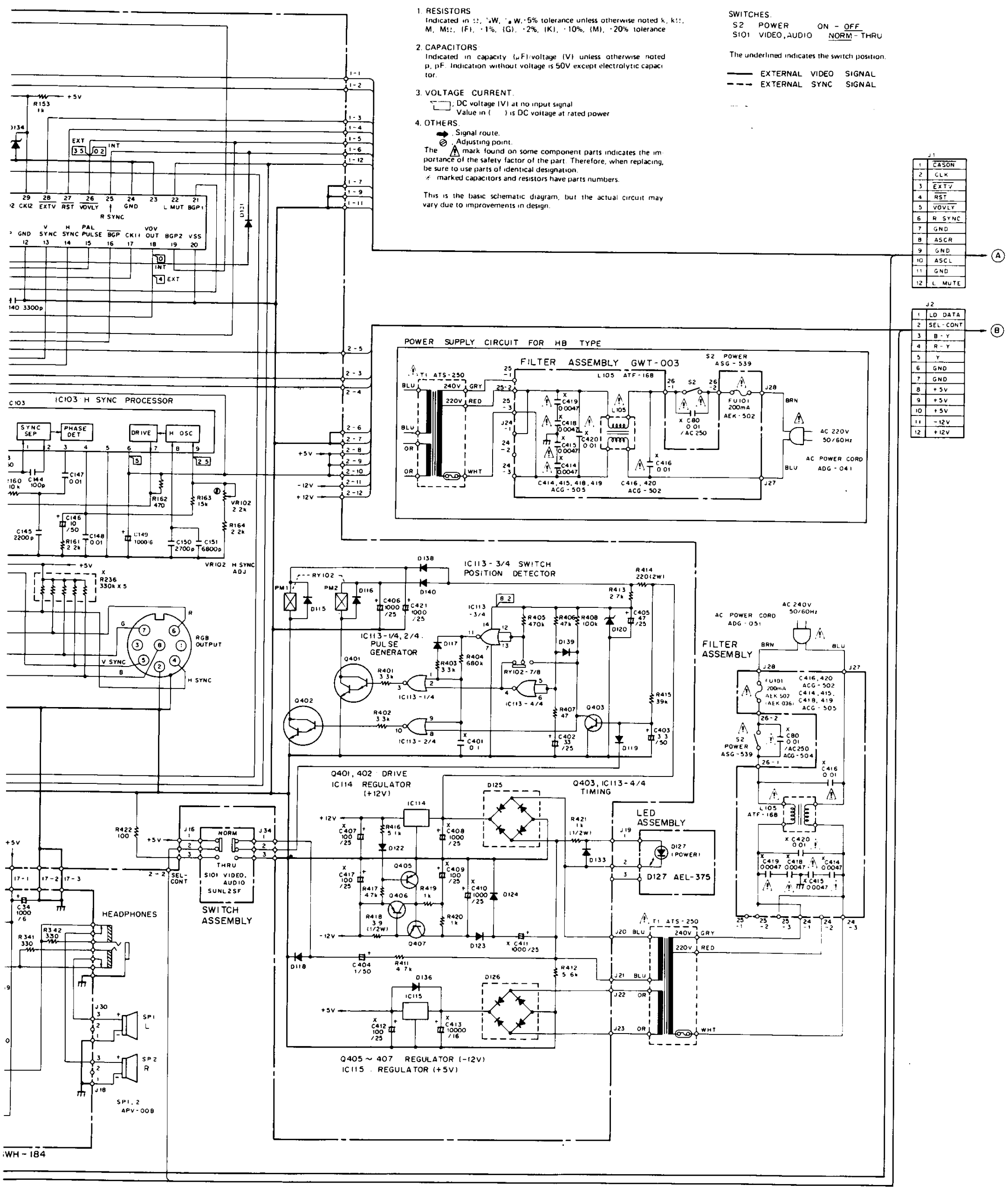
4. OTHERS.
➡ ; Signal route.
⊘ ; Adjusting point.
The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.
✗ marked capacitors and resistors have parts numbers.

This is the basic schematic diagram, but the actual circuit may vary due to improvements in design.

SWITCHES.
S2 POWER ON - OFF
S101 VIDEO, AUDIO NORM - THRU

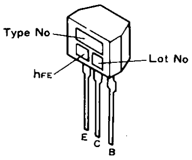
The underlined indicates the switch position.

——— EXTERNAL VIDEO SIGNAL
– – – EXTERNAL SYNC SIGNAL

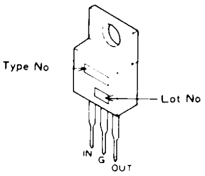


External Appearance of Transistors and ICs

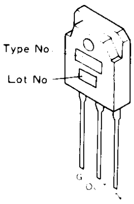
2SA933S
2SC1740S



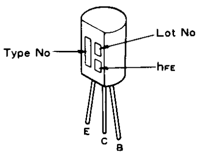
μPC78M08H
μPC7812H



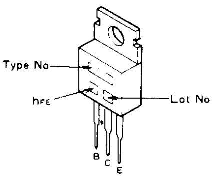
SI-3052V



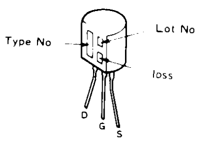
2SB560



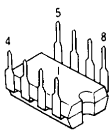
2SD836A



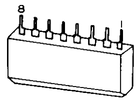
2SK117



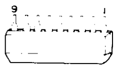
- 8 Pin
  M5218P
  SN75140P



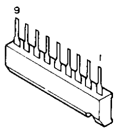
M5218L



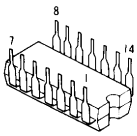
- 9 Pin
  AN5750
  AN6041



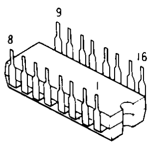
BA526



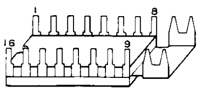
- 14 Pin
  SN74LS02N
  SN74LS30N
  SN74LS04N
  SN74LS32N
  SN74LS08N
  SN74LS05N
  SN74LS74AN
  SN74LS38N



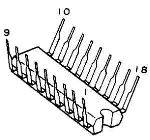
- 16 Pin
  M74LS30P
  SN74LS367AN
  SN74LS157N
  SN74LS139N
  SN74LS153N



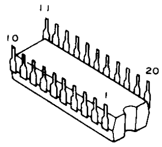
AN5620X



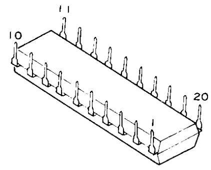
- 18 Pin
  TMS4416-15NL
  M5M4416P-15



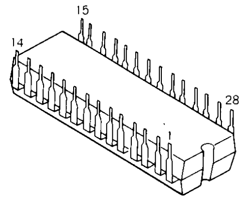
- 20 Pin
  SN74LS374N



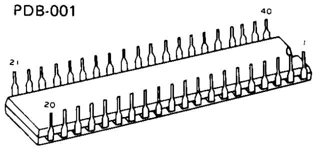
SN74LS245N



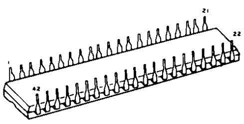
- 28 Pin
  M5L2764
  YM-2301-23908



- 40 Pin
  TMS9129NL
  LH0080A
  YM-2149
  M5L8255AP-5
  PDB-001

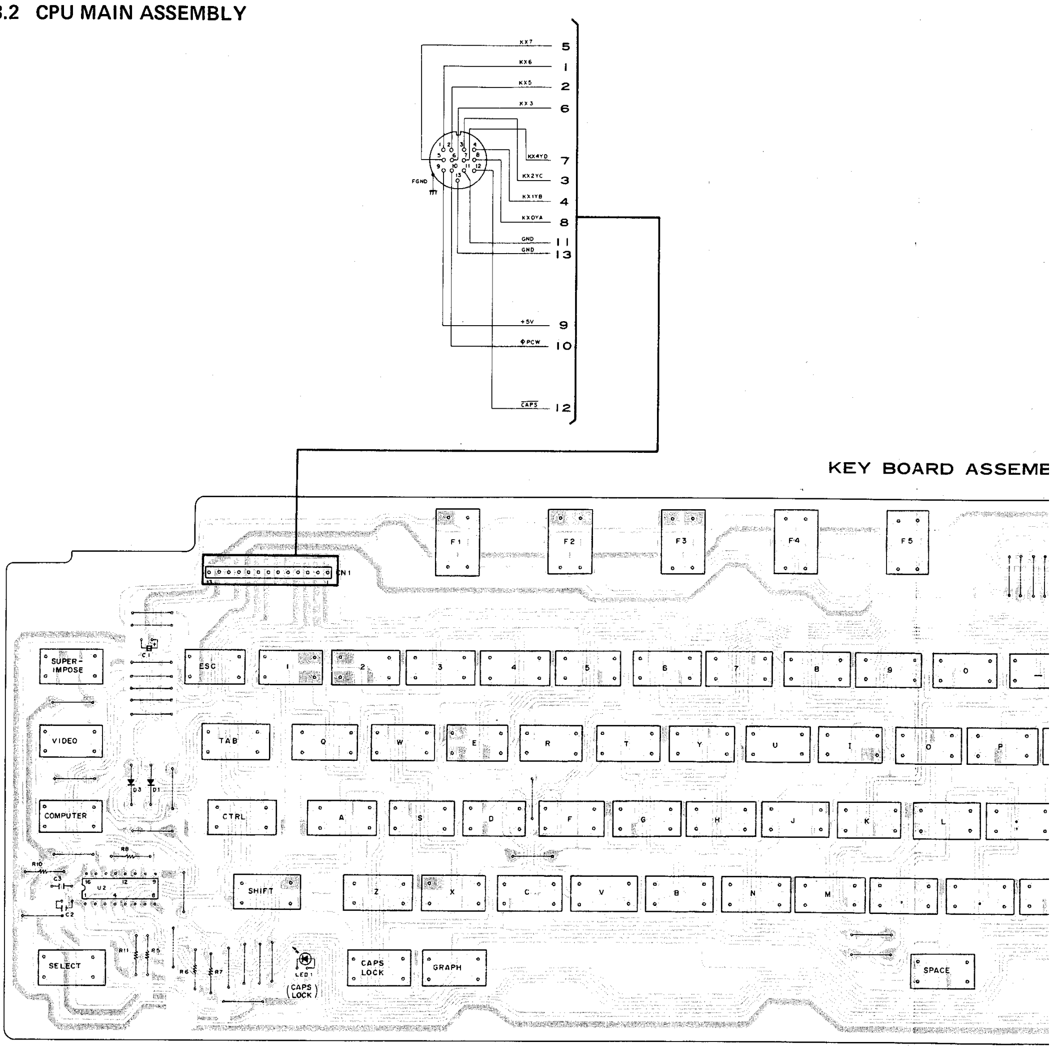


- 42 Pin
  MB111S112

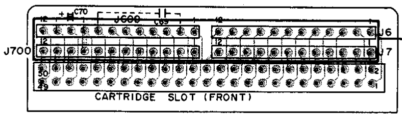


8.2 CPU MAIN ASSEMBLY

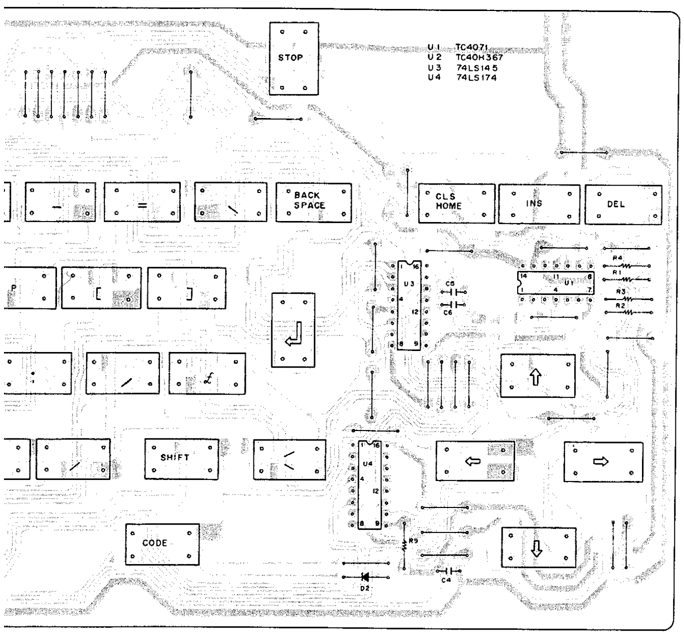
KEY BOARD ASSEME



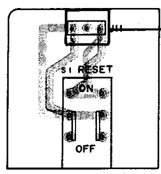
SLOT CONNECTOR ASSEMBLY



SEMBLY



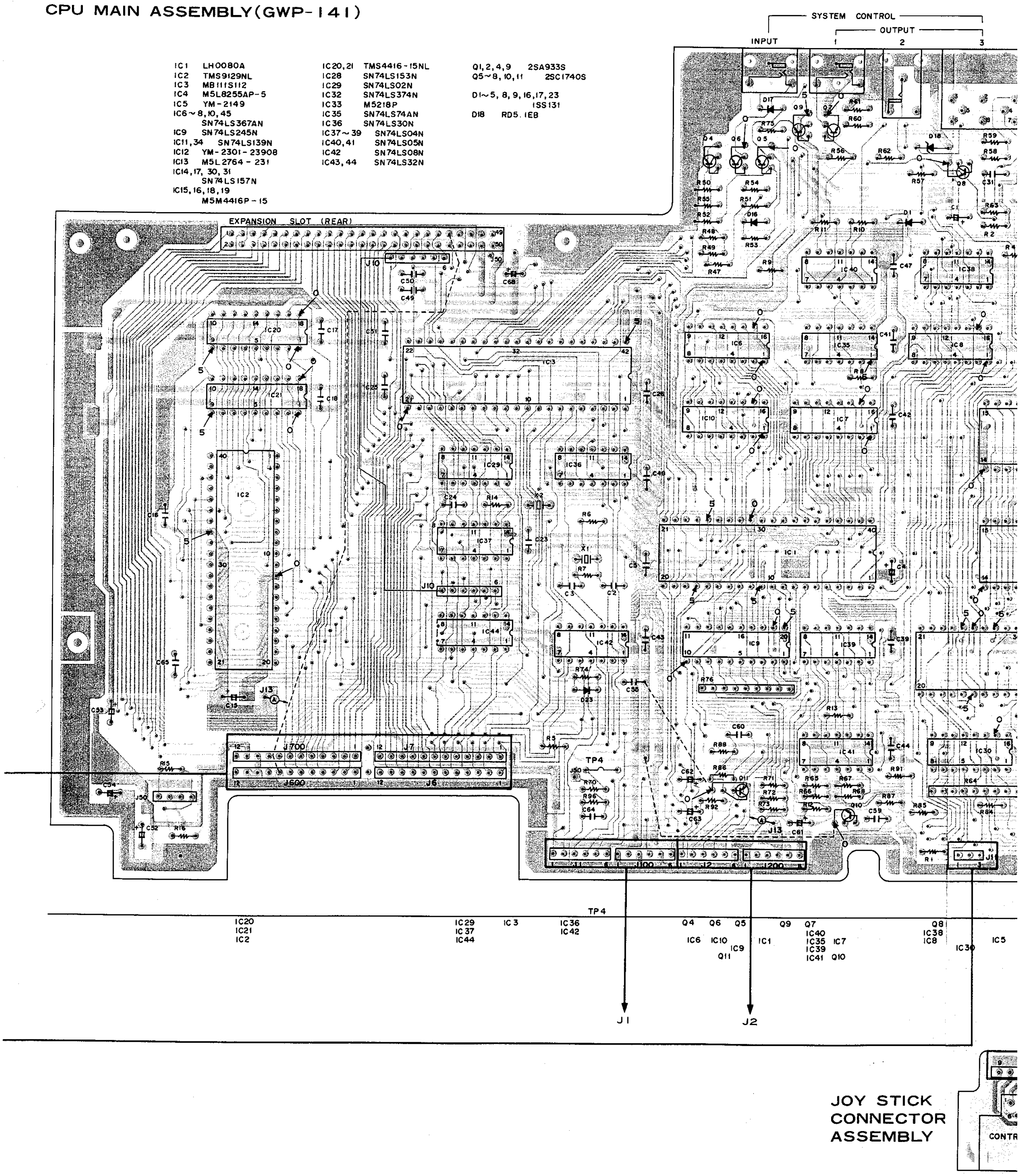
SWITCH ASSEMBLY



7 8 9

CPU MAIN ASSEMBLY(GWP-141)

IC1	LH0080A	IC20,21	TMS4416-15NL	Q1,2,4,9	2SA933S
IC2	TMS9129NL	IC28	SN74LS153N	Q5~8,10,11	2SC1740S
IC3	MB111S112	IC29	SN74LS02N	D1~5, 8, 9, 16, 17, 23	1SS131
IC4	M5L8255AP-5	IC32	SN74LS374N	D18	RD5.1EB
IC5	YM-2149	IC33	M5218P		
IC6~8,10,45	SN74LS367AN	IC35	SN74LS74AN		
IC9	SN74LS245N	IC36	SN74LS30N		
IC11,34	SN74LS139N	IC37~39	SN74LS04N		
IC12	YM-2301-23908	IC40,41	SN74LS05N		
IC13	M5L2764-231	IC42	SN74LS08N		
IC14,17,30,31	SN74LS157N	IC43,44	SN74LS32N		
IC15,16,18,19	M5M4416P-15				

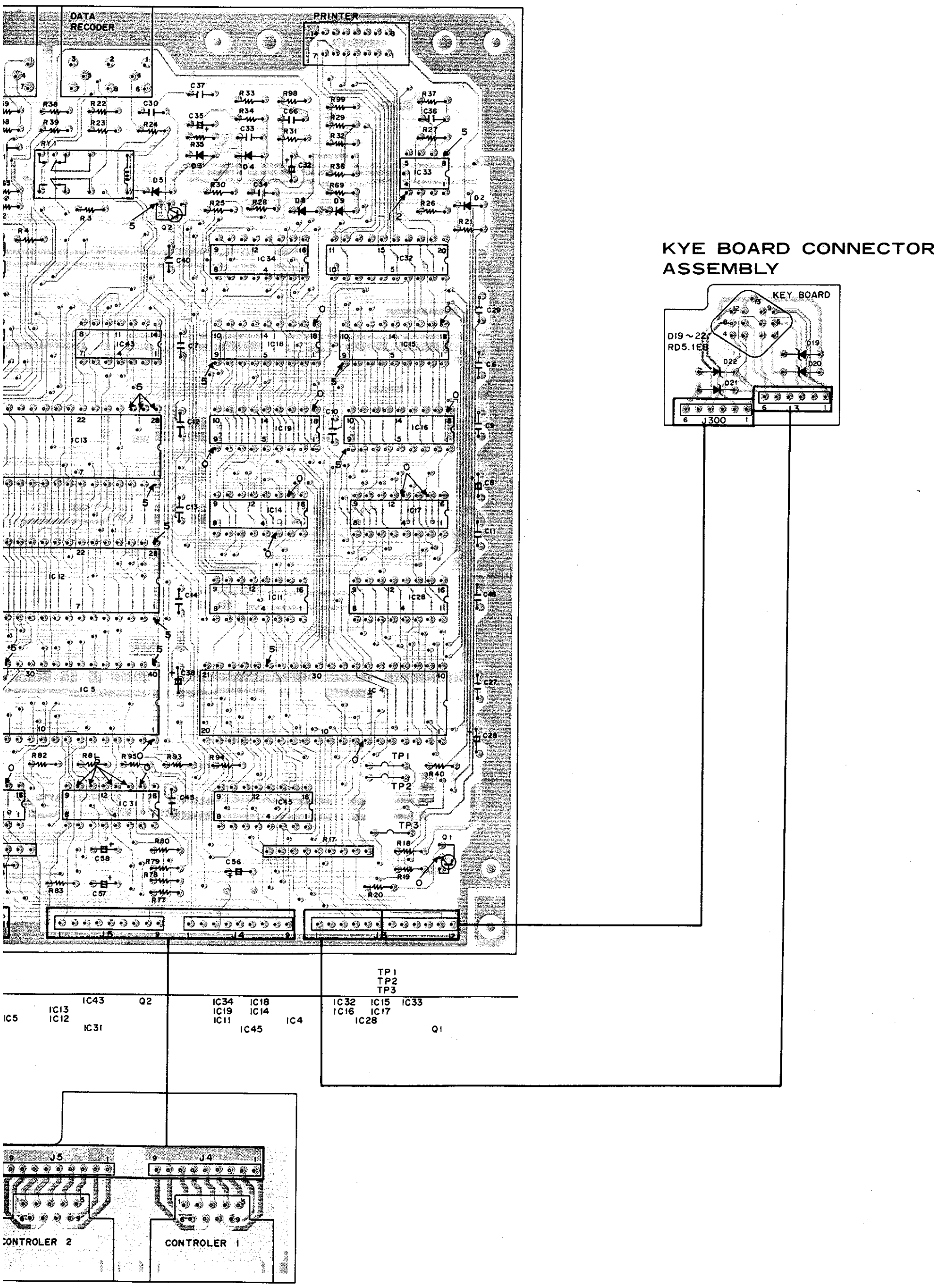


JOY STICK CONNECTOR ASSEMBLY

7 8 9

10 11 12

A

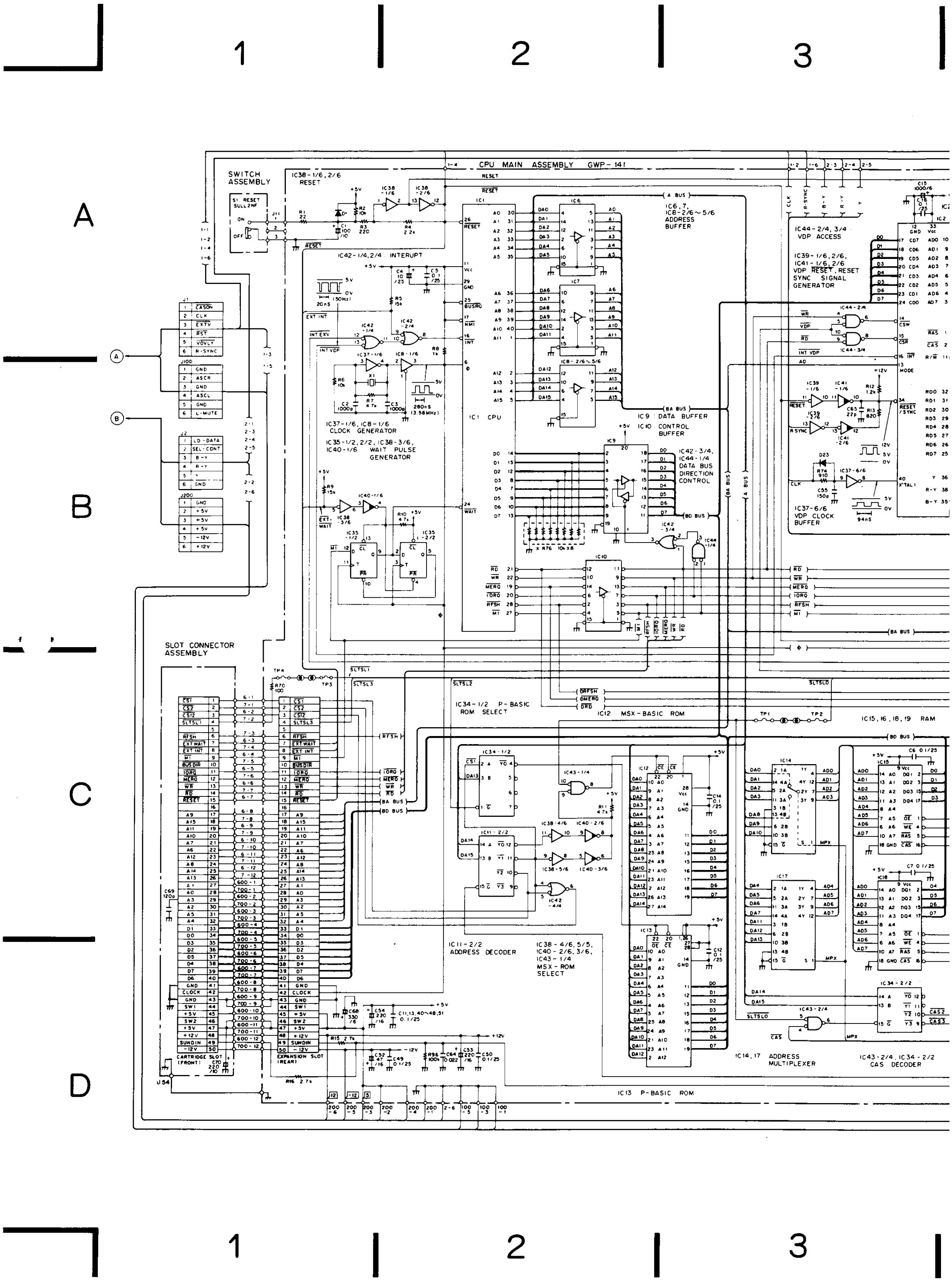


B

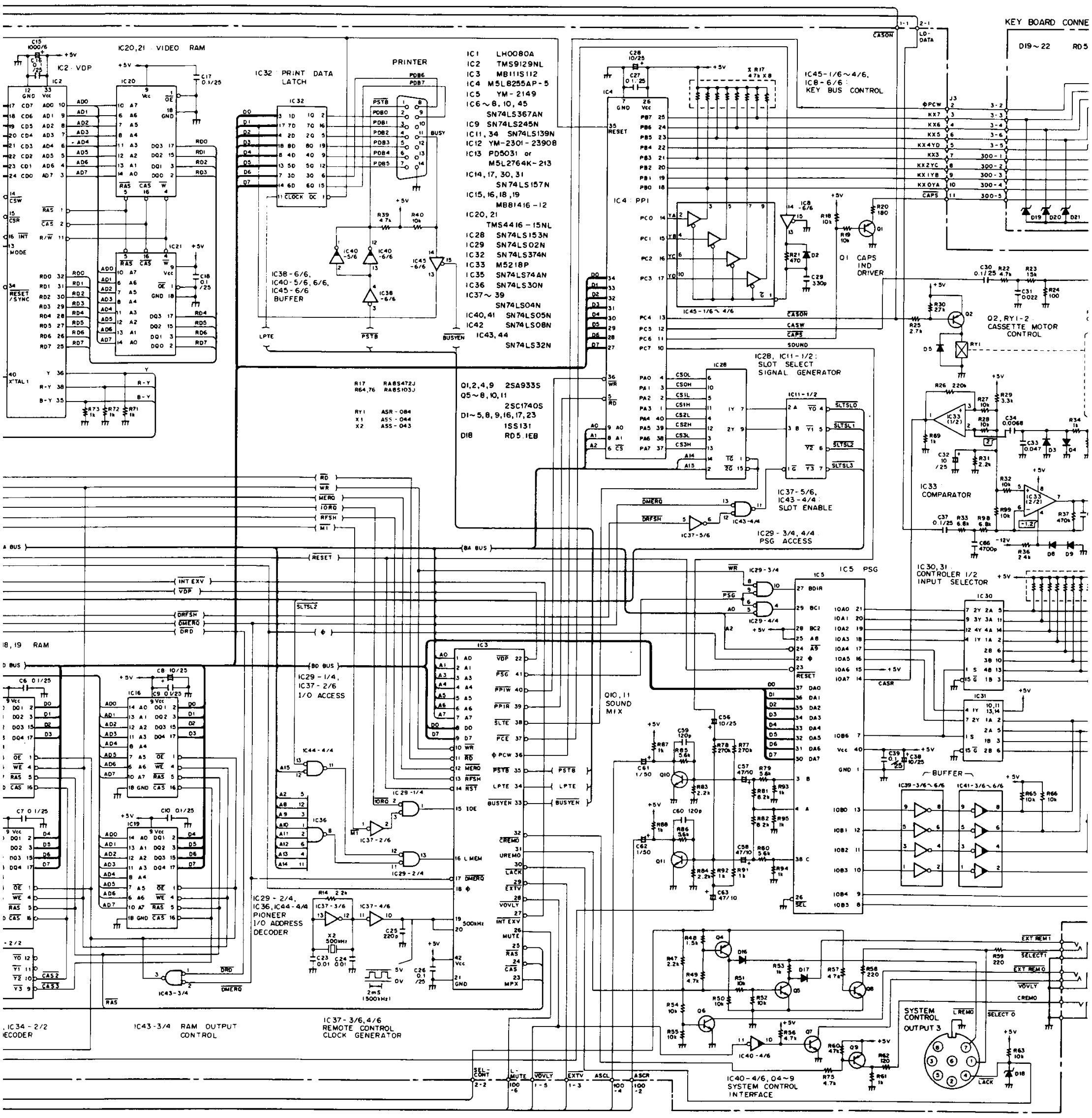
C

D

10 11 12

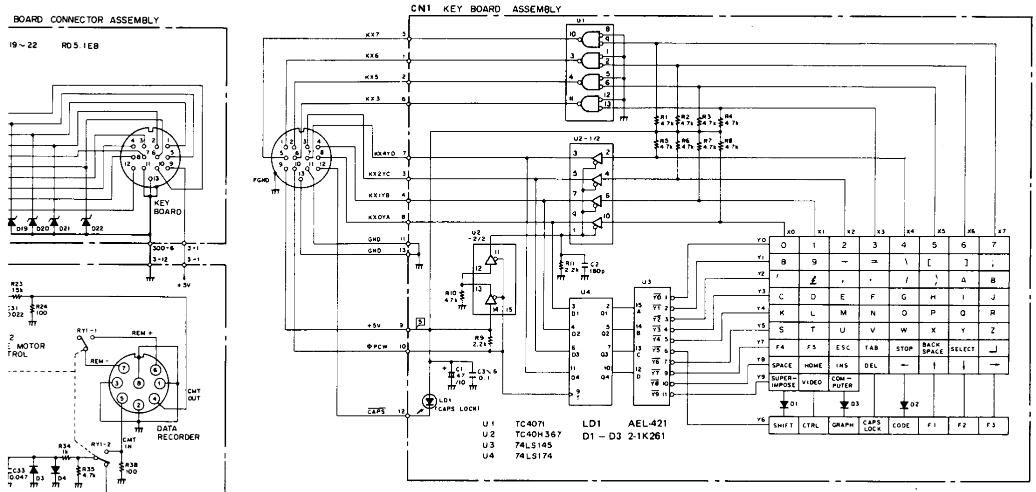

1
2
3
A
B
C
D
CPU MAIN ASSEMBLY GWP-141
SWITCH ASSEMBLY
IC38-1/6, 2/6 RESET
IC42-1/4, 2/4 INTERUPT
IC37-1/6, IC8-1/6 CLOCK GENERATOR
IC35-1/2, 2/2, IC38-3/6, IC40-1/6 WAIT PULSE GENERATOR
IC1 CPU
IC6, 7, IC8-2/6~5/6 ADDRESS BUFFER
IC9 DATA BUFFER
IC10 CONTROL BUFFER
IC42-3/4, IC44-1/4 DATA BUS DIRECTION CONTROL
IC44-2/4, 3/4 VDP ACCESS
IC39-1/6, 2/6, IC41-1/6, 2/6 VDP RESET, RESET SYNC SIGNAL GENERATOR
IC37-6/6 VDP CLOCK BUFFER
SLOT CONNECTOR ASSEMBLY
CARTRIDGE SLOT (FRONT)
EXPANSION SLOT (REAR)
IC34-1/2 P-BASIC ROM SELECT
IC12 MSX-BASIC ROM
IC11-2/2 ADDRESS DECODER
IC38-4/6, 5/6, IC40-2/6, 3/6, IC43-1/4 MSX-ROM SELECT
IC13 P-BASIC ROM
IC15, 16, 18, 19 RAM
IC14, 17 ADDRESS MULTIPLEXER
IC43-2/4, IC34-2/2 CAS DECODER

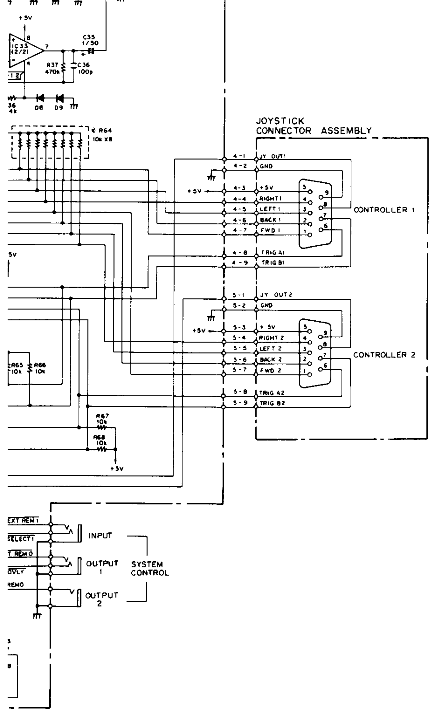
4 5 6



IC2 VDP
IC20,21 VIDEO RAM
IC32 PRINT DATA LATCH
PRINTER
IC1 LH0080A
IC2 TMS9129NL
IC3 MB111S112
IC4 M5L8255AP-5
IC5 YM-2149
IC6~8, 10, 45 SN74LS367AN
IC9 SN74LS245N
IC11, 34 SN74LS139N
IC12 YM-2301-23908
IC13 PD5031 or M5L2764K-213
IC14, 17, 30, 31 SN74LS157N
IC15, 16, 18, 19 MB81416-12
IC20, 21 TMS4416-15NL
IC28 SN74LS153N
IC29 SN74LS02N
IC32 SN74LS374N
IC33 M5218P
IC35 SN74LS74AN
IC36 SN74LS30N
IC37~39 SN74LS04N
IC40, 41 SN74LS05N
IC42 SN74LS08N
IC43, 44 SN74LS32N
Q1,2,4,9 2SA933S
Q5~8,10,11 2SC1740S
D1~5,8,9,16,17,23 1SS131
D18 RD5.1EB
IC4 PPI
IC45-1/6~4/6, IC8-6/6 KEY BUS CONTROL
KEY BOARD CONNE
IC28, IC11-1/2 SLOT SELECT SIGNAL GENERATOR
IC37-5/6, IC43-4/4 SLOT ENABLE
IC29-3/4, 4/4 PSG ACCESS
IC5 PSG
Q2, RY1-2 CASSETTE MOTOR CONTROL
IC33 COMPARATOR
IC30, 31 CONTROLER 1/2 INPUT SELECTOR
BUFFER
Q10, 11 SOUND MIX
IC29-1/4, IC37-2/6 I/O ACCESS
IC29-2/4, IC36, IC44-4/4 PIONEER I/O ADDRESS DECODER
IC43-3/4 RAM OUTPUT CONTROL
IC37-3/6, 4/6 REMOTE CONTROL CLOCK GENERATOR
IC40-4/6, Q4~9 SYSTEM CONTROL INTERFACE
SYSTEM CONTROL OUTPUT 3

4 5 6





1. RESISTORS
Indicated in Ω, ¼W, ⅙W, ±5% tolerance unless otherwise noted k, kΩ, M; MΩ, (F), ±1%, (G); ±2%, (K), ±10%, (M), ±20% tolerance

2. CAPACITORS.
Indicated in capacity (μF)/voltage (V) unless otherwise noted p, pF. Indication without voltage is 50V except electrolytic capacitor.

3. VOLTAGE
▭: DC voltage (V) at no input signal
Value in ( ) is DC voltage at rated power

4. OTHERS:
The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.
⚡ marked capacitors and resistors have parts numbers.

This is the basic schematic diagram, but the actual circuit may vary due to improvements in design.

SWITCHES
S1 RESET ON – OFF

The underlined indicates the switch position.

▷ Marked gates have open colector outputs

—— DATA BUS LINE (8D BUS)

A B C D

9.ELECTRICAL PARTS LIST

NOTES:

- *When ordering resistors, first convert resistance values into code form as shown in the following examples.*

  Ex. 1 When there are 2 effective digits (any digit apart from 0), such as 560 ohm and 47k ohm (tolerance is shown by J=5%, and K=10%).

560Ω	*56 × 10¹*	*561 .....*	*RD¼PS 561 J*
47kΩ	*47 × 10³*	*473 .....*	*RD¼PS 473 J*
0.5Ω	*0R5 ....*		*RN2H 0R5 K*
1Ω	*010 ....*		*RS1P 010 K*

  Ex. 2 When there are 3 effective digits (such as in high precision metal film resistors).

5.62kΩ	*562 × 10¹*	*5621 ....*	*RN¼SR 5621 F*

- *The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.*
- *For your Parts Stock Control, the fast moving items are indicated with the marks ★★ and ★.*

  ★★ GENERALLY MOVES FASTER THAN ★

  This classification shall be adjusted by each distributor because it depends on model number, temperature, humidity, etc.

Miscellaneous Parts List

Mark	Symbol	Description	Part No.
		Main assembly	GWM-419 (HB)
			GWM-434 (HE)
		Phone amplifier assembly	GWH-184
		Switch assembly	
		Filter assembly	
		Volume assembly	
		LED assembly	
		CPU main assembly	GWP-141
		Switch assembly	
		Slot connector assembly	
		Joy stick connector assembly	
		Key board connector assembly	
		Key board assembly	
⚠ ★	T1	Power transformer (240V)	ATS-250
⚠ ★★	S2	Push switch (POWER)	ASG-539
⚠ ★★	FU101	Fuse	AEK-036 (AEK-502)
⚠	C80	Capacitor (0.047/AC400V)	ACG-504
⚠		AC power cord	ADG-041
		Speaker	APV-008

Main Assembly (GWM-419 : HB)
(GWM-434 : HE)

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
★★	IC101	AN5620X
★★	IC103	AN5750
★★	IC107	AN6041
★★	IC110	M5218L
★★	IC012	PDB001
★★	IC104, IC105	SN75140P
★★	IC113	TC4001BP
★★	IC108	TC74HC4066P
★★	IC116	μPC78M08H
★★	IC114	μPC7812H
★★	Q105, Q201, Q210, Q243, Q303,	2SA933S
★★	Q304, Q405, Q406	
★★	Q407	2SB560 (A)
★★	Q101 – Q104, Q106, Q108 – Q110, Q112 – Q114, Q204 – Q209, Q211, Q212, Q240 – Q242, Q244 – Q246, Q280 – Q284, Q301, Q302, Q305, Q306, Q309 – Q312, Q314, Q403	2SC1740S
★★	Q401, Q402	2SD836A
★★	Q107, Q111	2SK117
★★	Q248 – Q250	2SA933S-R
★★	Q202, Q203, Q247	2SC1740S-R
★	D105	HZ4.7EB
★	D134	HZ5.1EB
★	D137	HZ6.2EB
★	D120	HZ8.2EB
★	D125	RB152-A
★	D126	RB402S
	D103 – D104, D106 – D108, D110 – D119, D122, D128, D129 – D132, D133, D138 – D140	US1035
★	D101	1SV147
★	D123, D124, D136	11E2
★	D102, D121, D109	1SS131

SWITCH

Mark	Symbol & Description	Part No.
★★	RY102 Plunger switch	ASR-085

COILS

Mark	Symbol & Description	Part No.
	L101, L104 Inductor	ATH-075
	L102 Inductor	ATH-113
	L103 Inductor	ATH-114

CAPACITORS

Mark	Symbol & Description	Part No.
	C139, C207 – C209, C217, C241, C344, C401 (0.1μ)	CKDYX104M25
	C413 (10000μ/16V)	ACH-392
	C408, C410, C411 (1000μ/25V)	ACH-393
	C407, C409, C412, C417 (100μ/25V)	:H-394
	TC101	ACM-019
	C211, C212, C214, C215	CCCCH560J50
	C144, C303, C304	CCCSL101J50
	C313, C314	CCCSL151J50
	C106, C121	CCCSL220J50
	C281	CCCSL390J50
	C113	CCCUJ050C50
	C116	CCCUJ100D50
	C135	CCCUJ101J50
	C131	CCCUJ150J50
	C245	CCCUJ180J50
	C132	CCCUJ270J50
	C114, C134	CCCUJ470J50
	C107, C247	CCCUJ820J50
	C112	CEANL010M50
	C115	CEANL100M16
	C120	CEANP3R3M50
	C202	CEAR15M50L
	C103, C128, C142, C206, C284, C301, C302, C305 – C308, C315, C316, C404	CEAS010M50
	C102, C133, C138, C143, C146, C201, C210, C242, C244, C282, C285, C311, C312, C323, C324, C340, C346	CEAS100M50
	C246, C290, C309, C310	CEAS101M10
	C406, C421	CEAS102M25
	C104, C204	CEAS221M10
	C403	CEAS3R3M50
	C109, C286, C402	CEAS330M25
	C240	CEAS331M10
	C243	CEAS4R7M50
	C213, C216	CEAS470M10
	C405	CEAS470M25
	C101, C280	CEAS471M10
	C317, C318	CKCYB102K50
	C105, C203	CKCYB222K50

Mark	Symbol & Description	Part No.
	C108	CKCYB331K50
	C205	CKCYB332K50
	C111, C119, C122, C123, C125 – C127, C136, C147, C287	CKCYF103Z50
	C110, C124, C137	CKCYF473Z50
	C129, C130, C148	CQMA103J50
	C117, C118	CQMA123J50
	C319, C320	CQMA153J50
	C145	CQMA222J50
	C150	CQMA272J50
	C140	CQMA332J50
	C141	CQMA472J50
	C151, C321, C322	CQMA682J50
	C345	CQMA823J50
	C149	CEAS102M6
	C152	CQMA273J50

RESISTORS

NOTE: When ordering resistors, convert the resistance value into code form, and then rewrite the part no. as before.

Mark	Symbol & Description	Part No.
★	VR104, VR106 Semi-fixed	VRTB6VS102
★	VR102, VR105, VR109 Semi-fixed	VRTB6VS222
★	VR101 Semi-fixed	VRTB6VS472
★	VR103 Semi-fixed	VRTB6VS101
	R414	RS2LMF221J
	R260, R262	RN1/4PQ6800F
	R236	RA5S331J
	R166	RD1/4PM225J
	R421	RD1/2PMFL102J
	R281, R418	RD1/2PMF □□□J
	Other resistors	RD1/8PM □□□J

OTHERS

Mark	Symbol & Description	Part No.
	Terminal	AKB-130
	IC socket (40P)	AKH-024
	DIN socket (RGB OUT)	AKP-085
	BNC socket (VIDEO OUTPUT)	AKX-204
	BNC socket (VIDEO INPUT)	AKX-205
★	X101 crystal resonator	ASS-041
	RF modulator	AXX-015 (HB) AXX-014 (HE)
	Sheet	AEP-056
	Screw	ABA-234
	Screw	ABA-284
	Screw	PBZ30P060FMC

Filter Assembly

FILTER

Mark	Symbol & Description	Part No.
	L105 Line Filter	ATF-168

CAPACITORS

Mark	Symbol & Description	Part No.
	C416, C420	ACG-502
	C414, C415, C418, C419	ACG-505

Phone Amplifier Assembly (GWH-184)

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
★★	IC111, IC112	BA526

CAPACITORS

Mark	Symbol & Description	Part No.
	C325, C326	CEASR47M50
	C341	CEAS102M6
	C331, C332	CEAS221M10
	C327 – C330	CEAS470M10
	C335, C336	CEAS471M6
	C333, C334	CKCYB222K50

RESISTORS

NOTE: When ordering resistors, convert the resistance value into code form, and then rewrite the part no. as before.

Mark	Symbol & Description	Part No.
	All resistors	RD1/8PM □□□J

OTHERS

Mark	Symbol & Description	Part No.
	Terminal (HEADPHONE)	AKN-056

Volume Assembly

RESISTORS

Mark	Symbol & Description	Part No.
★	VR107 Slide volume (100k)	ACX-142
★	VR108 Slide volume (50k)	ACX-143

LED Assembly

SEMICONDUCTOR

Mark	Symbol & Description	Part No.
★	D127	AEL-375

Switch Assembly

SWITCH

Mark	Symbol & Description	Part No.
★★	S101 Push switch	SUNL2SF

CPU Main Assembly (GWP-141)

Mark	Symbol & Description	Part No.
★★	IC1	LH0080A
★★	IC3	MB111S112
★★	IC13	PD5031
★★	IC4	M5L8255AP-5 (μPD8255AC-2)
★★	IC15, IC16, IC18, IC19	MB81416-12 (M5M4416P-15)
★★	IC33	M5218P
★★	IC29	SN74LS02N (M74LS02P)
★★	IC37 – IC39	SN74LS04N (M74LS04P)
★★	IC40, IC41	SN74LS05N (M74LS05P)
★★	IC42	SN74LS08N (M74LS08P)
★★	IC11, IC34	SN74LS139N (M74LS139P)
★★	IC28	SN74LS153N (M74LS153P)
★★	IC14, IC17, IC30, IC31	SN74LS157N (M74LS157P)
★★	IC9	SN74LS245N (M74LS245P)
★★	IC36	SN74LS30N (M74LS30P)
★★	IC43, IC44	SN74LS32N (M74LS32P)
★★	IC6 – IC8, IC10, IC45	SN74LS367AN (M74LS367AP)
★★	IC32	SN74LS374N
★★	IC35	SN74LS74AN
★★	IC20, IC21	TMS4416-15NL (M5M4416P-15)
★★	IC2	TMS9129NL
★★	IC5	YM-2149
★★	IC12	YM-2301-23908
★★	Q1, Q2, Q4, Q9	2SA933S
★★	Q5 – Q8, Q10, Q11	2SC1740S
★	D18	RD5.1EB
★	D1 – D5, D8, D9, D16, D17, D23	1SS131

SWITCH

Mark	Symbol & Description	Part No.
★★	RY1	ASR-084

CAPACITORS

Mark	Symbol & Description	Part No.
	C5 – C7, C9 – C14, C16 – C18, C26, C27, C30, C37, C39, C40 – C51	CKDYX104M25
	C36, C55	CCCCH151J50
	C59, C60	CCCSL12150
	C65	CCCSL220J50
	C25	CCCSL221J50
	C35, C61, C62	CEAS010M50
	C4, C8, C28, C32, C37, C38, C56	CEAS100M25
	C1	CEAS101M10
	C15	CEAS102M6
	C53, C54	CEAS221M16
	C57, C58, C63	CEAS470M10
	C52	CEAS470M16
	C2, C3	CKCYB102K50
	C23, C24	CKCYB103K50
	C29	CKCYB331K50
	C31, C64	CKCYF223Z50
	C33	CKCYF473Z50
	C66	CQMA472J50
	C34	CQMA682J50
	C68	CEAS331M6
	C70	CEAS221M10
	C36	CCCH101J50
	C59, C69	CCDSL121J50

RESISTORS

Mark	Symbol & Description	Part No.
	R17, R64, R76	RA8S □□□J
	Other resistors	RD1/8PM □□□J

OTHERS

Mark	Symbol & Description	Part No.
	IC socket (28P)	AKH-018
	IC socket (40P)	AKH-024
	Terminal	AKN-206
	Terminal	AKN-207
	DIN socket (DATA RECORDER)	AKP-085
	DIN socket (OUTPUT 3)	AKP-086
	Socket (14P) (PRINTER)	AKP-087
	Socket (50P) (EXPANSION SLOT)	AKP-088
	X1 ceramic resonator	ASS-044
	X2 ceramic resonator	ASS-043
	Screw 3 x 10	BBZ30P100FZK
	Screw 3 x 8	VBZ30P080FZK
	Screw 4 x 8	VBZ40P080FZK

Switch Assembly

SWITCH

Mark	Symbol & Description	Part No.
★★	S1 Push switch (RESET)	SULL2NF

Slot Connector Assembly

OTHERS

Mark	Symbol & Description	Part No.
	Socket (50P) (CARTRIDGE SLOT)	AKP-088
	Screw 3 x 10	BBZ30P100FZK

Joy Stick Connector Assembly

OTHERS

Mark	Symbol & Description	Part No.
	Socket (9P)	AKP-089

Key Board Connector Assembly

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
★	D19 – D22	RD5.1EB

OTHERS

Mark	Symbol & Description	Part No.
	DIN socket (13P)	AKP-074

Key Board Assembly

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
	U1	μPD4071BC
	U2	TC40H367P
	U3	SN74LS145N
	U4	SN74LS174N
	LD1	AEL-421
	D1 – D3	2-1K261

SWITCHES

Mark	Symbol & Description	Part No.
	Tact switch	ASG-161
	Soft push switch	AZS-010

CAPACITORS

Mark	Symbol & Description	Part No.
	C3 – C6 0.1μF/16V	CKDYX104M25
	C1 47μF/16V	CEAS470M16
	C2 180pF/50V	CCDSL181J50

RESISTORS

Mark	Symbol & Description	Part No.
	R9, R11	RD1/4PM222J
	R1 – R8, R10	RD1/4PM472J

10. ADJUSTMENTS

1. G Overlay Adjustment
2. R • B Adjustment
3. Horizontal Position Adjustment
4. Color Subcarrier Frequency Adjustment
5. Color Subcarrier Suppression Adjustment
6. Black Level Adjustment
7. Switching Spike Elimination Adjustment
8. Hue Adjustment
9. Confirmation by Check ROM

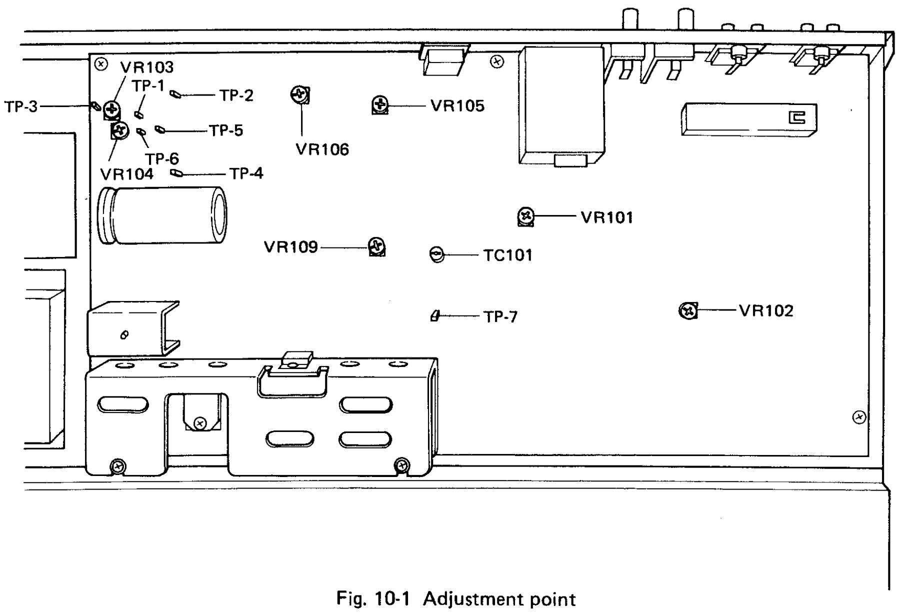


Fig. 10-1 Adjustment point

10.1 G OVERLAY ADJUSTMENT

1. Connect the measuring equipment outlined in Fig. 10-2 to PX-7.
2. Set the monitor TV to RGB input.
3. Switch the PX-7 power on, and then with the initial message on display (see Fig. 10-3) press the return key.
4. When the next message is displayed (see Fig. 10-4), press [1] to select MSX+P-BASIC.
5. Connect a digital voltmeter to TP-3.
6. Run the sample program given in Fig. 10-5 for output of color bars on the TV screen.
7. Turn VR104 fully clockwise.
8. Adjust VR103 to obtain the green color bar arrangement shown in Fig. 10-6.
9. Then slowly turn VR103 counter clockwise, and record the TP-3 voltage A when noise becomes apparent in the bars.
10. Next turn VR103 slowly clockwise, and again record the TP-3 voltage B when noise becomes apparent in the bars.
11. Finally adjust VR103 to obtain the TP-3 voltage which is half way between voltages A and B.

P-BASIC Version 1.1
Copyright 1985 by PIONEER
*** BASIC MODE SELECT ***
[1] MSX BASIC + P-BASIC
[2] MSX BASIC
PUSH [1] or [2]

(White characters on blue background)

Fig. 10-4 Message 2

```
10  REM
20  SCREEN 2: COLOR, Ø , Ø
    : CLS
30  FOR X=Ø TO 255
    STEP 16
40. LINE (X, 95) – (X+15),
    191), X/16, BF
50  NEXT X
60  FOR X=Ø TO 255
    STEP 16
70  LINE (X,Ø) – (X+1, 95),
    X/16, BF
80  NEXT X
90  GOTO 90
```

Fig. 10-5 Sample program

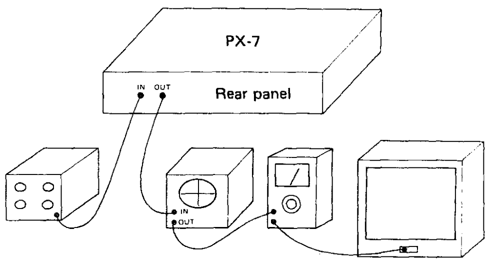


Fig. 10-2 Connections

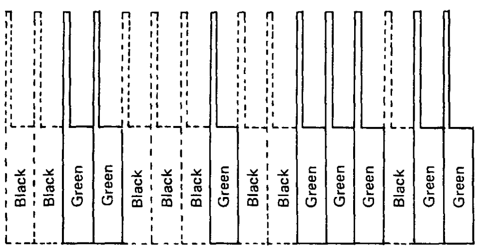


Fig. 10-6 G overlay adjustment

MSX system
virsion 1.0
Copyright 1983 by Microsoft

(White characters on blue background)

Fig. 10-3 Message 1

10.2 R-B ADJUSTMENT

1. Connect a digital voltmeter to TP-6.
2. Adjust VR104 to obtain the color bar arrangement shown in Fig. 10-7.
3. Slowly turn VR104 counter closkwise, and record the TP-6 voltage C when noise becomes apparent in the color bars.
4. Next turn VR104 slowly clockwise, and again record the TP-6 voltage D when noise becomes apparent in the bars.
5. Finally adjust VR104 to obtain the TP-6 voltage which is half way between voltages C and D.

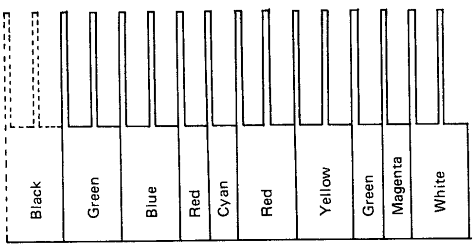


Fig. 10-7 Adjustment

10.3 HORIZONTAL POSITION ADJUSTMENT

1. Press the COMP key to display the computer mode screen with the color bar output (see Fig. 10-7).
2. Then press the SUPERIMPOSE key to obtain a composite display. Compare the color bars in this composite screen with the color bars in the previous computer mode screen, and adjust VR102 during the composite screen display to keep the color bar displacement in the horizontal direction within the width of the narrow color bar (see Fig. 10-8).

(Monitor TV screen same as in R-B adjustment)

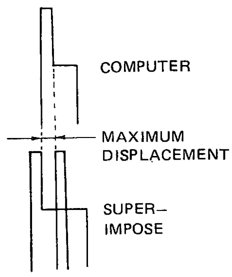


Fig. 10-8

10.4 COLOR SUBCARRIER FREQUENCY ADJUSTMENT

1. Connect a frequency counter to TP-7.
2. Set the monitor TV to video input.
3. Run the sample program shown in Fig. 10-5 for output color bars on the TV screen.
4. After first pressing the SUPERIMPOSE key to switch PX-7 to composite screen display, press the COMP key to switch to computer mode.
5. Adjust TC101 to obtain a reading of 4.433600 MHz ±20Hz in the frequency counter.

10.5 COLOR SUBCARRIER SUPPRESSION ADJUSTMENT

Adjusting with a vectorscope

1. Switch to computer mode (by pressing the COMP key).
2. Connect the vectorscope as indicated in Fig. 10-9.
3. Adjust VR106 so that the origins a and a' of the two reflected burst vectors coincide with each other (see Photo. 10-1).

Adjusting without a vectorscope (rough adjustment)

1. Connect an oscilloscope to the VIDEO OUT terminals with the PX-7 in computer mode. Observe the video synchronizing signal.
2. Adjust VR106 to minimize the carrier which is superimposed on the video synchronizing signal (see Photo. 10-2).

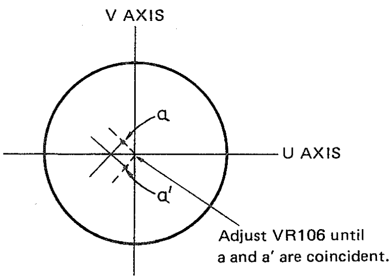


Fig. 10-9 Color subcarrier suppression adjustment

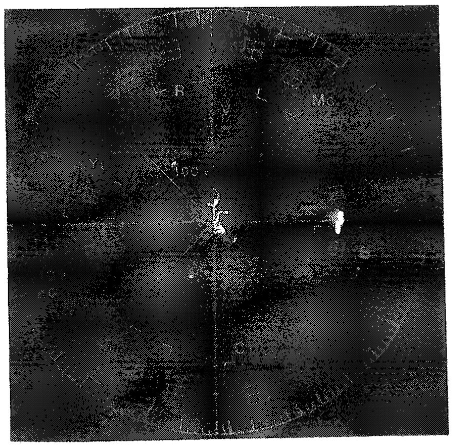


Photo. 10-1

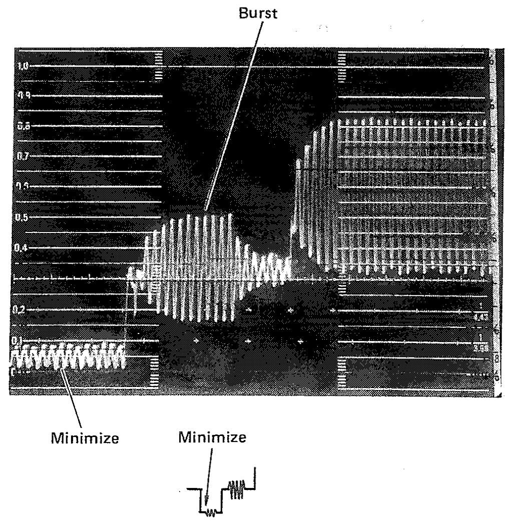


Photo. 10-2

10.6 BLACK LEVEL ADJUSTMENT

1. Press the SUPERIMPOSE key to switch to composite mode.
2. Check that the external video signal output level lies within the 1Vp-p±10% range.
3. Adjust VR105 to align the internal black level shown in Fig. 10-10 with the external pedestal level (center of switching spike).

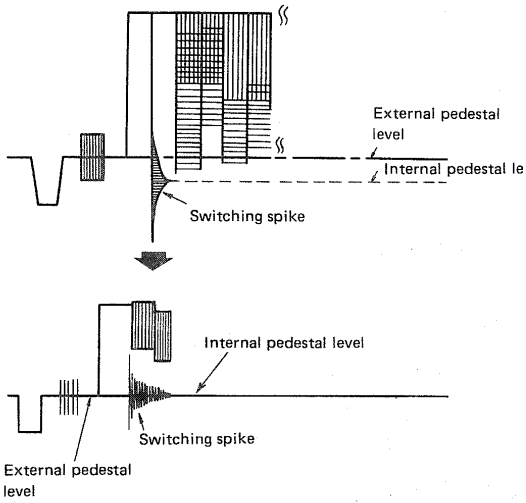


Fig. 10-10 Black level adjustment

10.7 SWITCHING SPIKE ELIMINATION ADJUSTMENT

1. Switch to composite mode, and observe the VIDEO OUT terminal output in an oscilloscope.
2. Adjust VR109 to minimize the switching spike in the composite video signal (see Fig. 10-11).

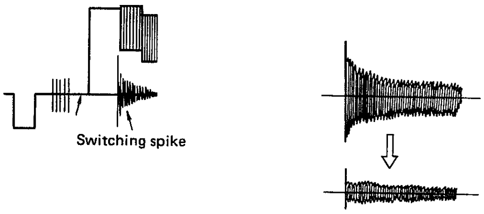


Fig. 10-11 Switching spike elimination adjustment

10.8 HUE ADJUSTMENT

Proceed with this adjustment only after the power has been on for at least five minutes.

Adjusting with a vectorscope

1. Press the SUPERIMPOSE key to switch to composite mode.
2. Enter the COLOR 4,4,4 input, and press the return key to obtain an all-blue screen.
3. Adjust VR101 $(0 \sim 0' \leq 2^\circ)$ so that the blue hue output obtained from the computer is symmetrical about the U axis as indicated in Fig. 10-13, and make sure that the external signal burst is fully coincident with the vectorscope burst point.

Adjusting without a vectorscope (rough adjustment)

1. Press the SUPERIMPOSE key to switch to composite mode.
2. Enter the COLOR 4,4,4 input, and press the return key to obtain an all-blue screen.
3. Connect an LD to VIDEO IN, adjust operating mode to STILL, and adjust VR101 to obtain a stable blue color in that screen.

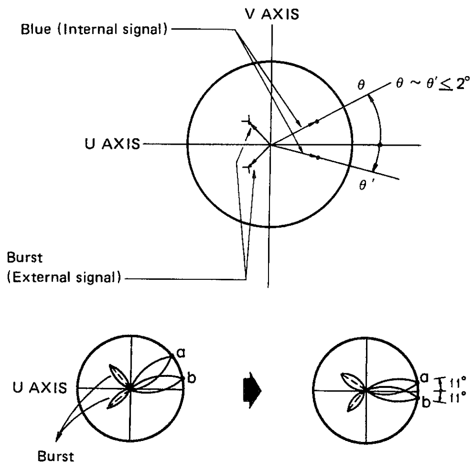


Fig. 10-12 Hue adjustment

11. INSPECTION ROM INSTRUCTION MANUAL

11-1 GENERAL OUTLINE

The PX-7 Inspection ROM Cartridges are jigs designed to efficiently analyze Palcom PX-7 [BK] / HB/HE failures. The two types of cartridges employed are: —

A. INSPECTION 1 FOR PX-7[BK] (UK[HB/HE]) VERSION

B. INSPECTION 2 FOR PX-7[BK] (UK[HB/HE]) VERSION

These two cartridges are used in the following way.

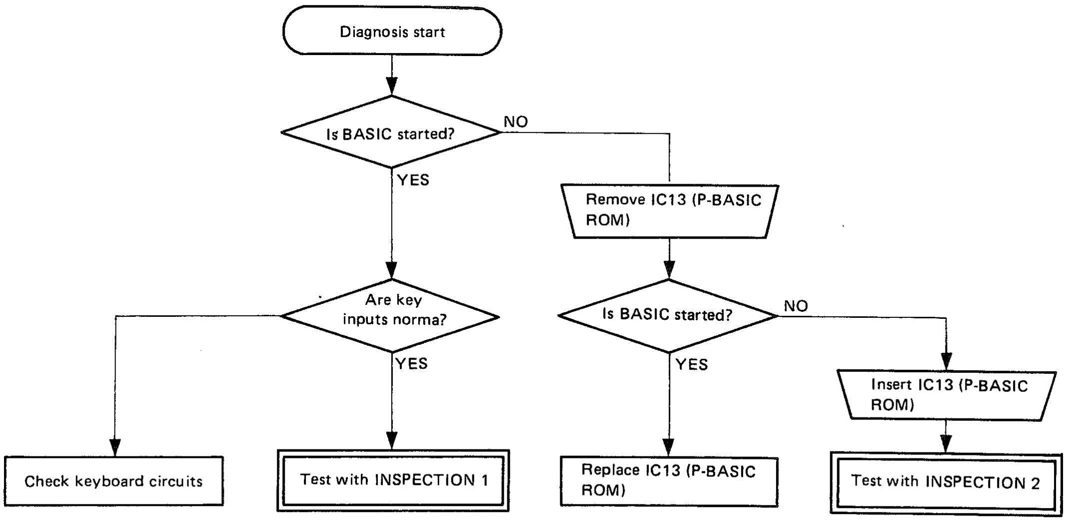


Fig. 11-1 Check

[1] Connect the display unit to the PX-7 and switch the power on with nothing loaded in the cartridge slot. Check that BASIC is started up (with output of the initial display which then switches to the BASIC mode select display). After selecting a mode by keyboard input, key in a suitable character to check for normal key input. If key inputs are normal, switch the power off, and insert the INSPECTION 1 cartridge into the cartridge slot in the front of the unit to commence the test.

[2] If BASIC fails to start, open the bonnet and remove IC13 (P-BASIC ROM) from its IC socket. Repeat the start procedure to see if BASIC will start up or not. (The BASIC mode select display is not obtained in this case — the same display as when MSX BASIC is selected (push key [2]) is obtained instead). If BASIC is started, replace the defective IC13 component.

[3] If BASIC still fails to start with IC13 removed, re-insert the component into the IC socket and load the INSPECTION 2 cartridge in the cartridge slot in the front of the unit to commence the test.

11-2 INSPECTION 1

The INSPECTION 1 program consists of BASIC (including P-BASIC commands) and machine language programs, and is located in 8000H thru BFFFH (16K bytes) in slot #1 (in front panel).
* Inserting the program in SLOT #3 (in rear panel) results in "syntax error" and failure to operate normally.

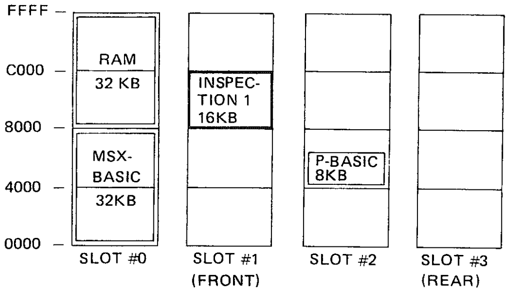


Fig. 11-2 Memory map

[1] The basic mode consists of MSX-BASIC and P-BASIC mode being selected by pressing key [1]. If key [2] is pressed to select only MSX-BASIC mode, the screen mode keys (SUPERIMPOSE, VIDEO and COMPUTER) cannot be used, and the system control test (6) cannot be executed. All other tests, however, can be executed.

[2] There are seven tests (0) thru (6). The desired test is selected by pressing the numerical key corresponding to that test on the menu screen.

[3] When a test (1) thru (6) is executed, the program returns to the menu screen upon completion of the test, or when the SPACE key is pressed.

[4] The aging test (0) consists of a loop test executed in the following sequence:

→ RAM test → ROM test → V-RAM test → video test → sound test ┐

To quit this loop and executed another test, either press the RESET button to return to the BASIC MODE SELECT menu, or press the CTRL and STOP keys to execute a program break, followed by re-executing by pressing the F5 key (RUN↵).

[5] The CTRL + STOP , SUPERIMPOSE , VIDEO , and COMPUTER keys are valid anywhere within this program while it is being run.
* Note, however, that the screen mode keys are only valid when the precaution described in [1] is observed.

[6] All tests proceed in accordance with messages displayed on the screen.

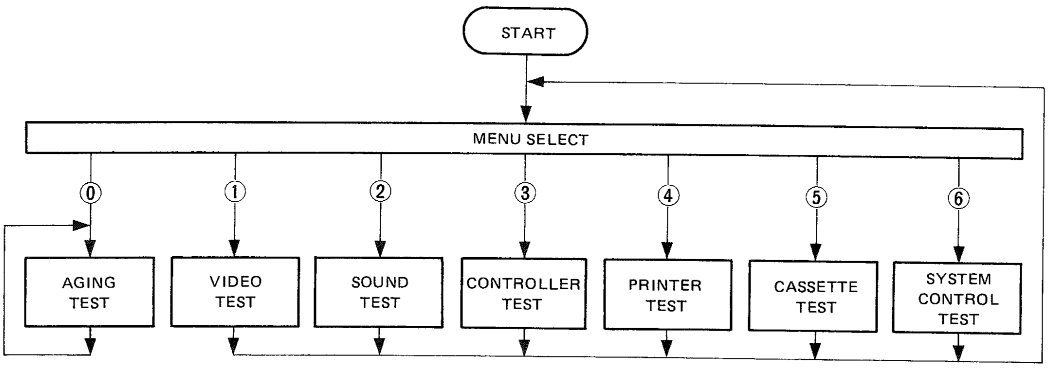


Fig. 11-3 Menu

Test Details

(0) Aging Test

[RAM TEST]
00H, 55H AAH, and FFH data is written within the C000H thru DFFFH and 8000H thru BFFFH RAM address ranges, and the written data is subsequently checked to see that it matches the read data.

* Since the E000H thru FFFFH address range forms the BASIC work area, it cannot be checked by this test. The INSPECTION 2 cartridge must be used if a check is desired.

[ROM TEST]

1. The total sum of data in all addresses (0000H thru 7FFFH) in the MSX-BASIC ROM (IC12) is checked to see that it comes to 2DH (check sum, or addition of all bytes excluding carry).
2. The total sum of data in all addresses (4000H thru 5FFFH) in the P-BASIC ROM (IC13) is checked to see that it comes to FFH.

[VRAM TEST]
00H, 55H, AAH and FFH data is written within the 3800H thru 3A98H VRAM address range, and is then compared with the read data.

* Since the screen settings would be destroyed, it is not possible to check all addresses by this test. Again, the INSPECTION 2 cartridge must be used if a check is desired.

[VIDEO TEST]
First the 16 color bar, and then "all white", are displayed on the screen.

[SOUND TEST]
The L channel, R channel, and center sounds are generated in that order.

(1) Video Test

The "16 color bar", "16 half bar", "all white", and "all blue" screen displays can be selected by numeral key input. This test is used in video system adjustments.

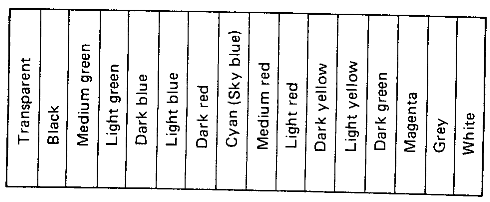
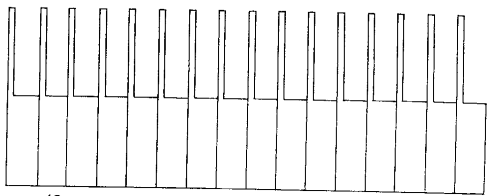


Fig. 11-4 16 color bar



(Same color arrangement as in the 16 color bar)

Fig. 11-5 16 half bar

(2) Sound Test

Testing of the following keys.

[1] L channel	PSG(IC5) B ch. (PIN 3) output check
[2] R channel	PSG(IC5) C ch. (PIN 38) output check
[3] Center (PSG)	PSG(IC5) A ch. (PIN 4) output check
[4] Center (PPI)	PSG(IC4) SOUND (PIN 10) output check (Low volume level)
[5] MUTE OFF NOTE 1	External audio input muting OFF
[6] Center (FILTER)	Center localization output frequency changed in cycles from 1 kHz to 10 kHz, 28 kHz and back to 1 kHz.
[7] Melody	Melody play

(3) Controller Test

Testing of CONTROLLER 1 and CONTROLLER 2 port.

Connect PX-JY8 to the selected CONTROLLER port.

1. The graphic characters shown in the accompanying diagram are shifted (and leave a trail) depending on the direction of the grip (but cannot be moved beyond the edge of the screen).

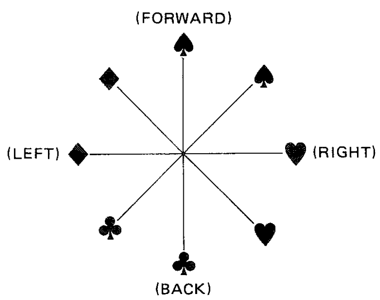


Fig. 11-6 Controller test

2. A beep sound is generated when trigger A (orange button in top of grip) is pressed, and the graphic character color is changed sequentially from COLOR 1 thru COLOR 15.
3. When trigger button B (grey button in the main unit) is pressed, a lower pitch sound (than the above beep sound) is generated, and the background color is changed from COLOR 1 thru COLOR 15. The graphic characters displayed on the screen are cleared at this stage and returned to the center position.

* Since the graphic characters cannot be distinguished if the character and background colors are the same, change either color by trigger operation.

(4) Printer Test

Output of the following characters to printer or CENTRONICS CHECK BOARD.

* If the CENTRONICS CHECK BOARD is used, ASCII codes 20H thru 7AH are shown in binary.
!"#$%&'()*+,–./0123456789:;<=>? @ABCDEFG
HIJKLMNOPQRSTUVWXYZ [\]^_` abcdefghij
klmnopqrstuvwxyz

(5) Cassette Test

Save data on cassette tape, and then load the tape and compare the data.

(6) System Cont Test

[1] SYSTEM CONT1 (SD-26)

Switch the INPUT selector to the TV position by remote control, and change the channel upwards.

- Do not change channels upwards if no external video signal is applied to the PX-7.
- Execute the remote control operation via SD-R5 (RGB pack)/ZE (see I/M for connection details).

[2] SYSTEM CONT2 (LD-1100)

[3] SYSTEM CONT3 (LD-700)

Activate the LV player, search for frame 1000, and then "step forward".

*Use CAV disc

NOTE 1

This MUTE OFF test must be done in COMPUTER mode. In case the picture is unstable because of the asyhchronbus (SUPERIMPOSE MODE, VIDEO MODE), push the COMPUTER key to recover the normal picture.

CPU Ass'y (AWP-022) TP1 Thru TP4 Functions

Description of the functions of TP1 thru TP4 mounted on the PX-7/HB, HE CPU ass'y (AWP-022) and the associated jumper-land JPA thru JPD).

- Under normal conditions, respective soldering of JPA thru JPD forms bridge short circuits where the MSX-BASIC ROM and 32K byte RAM become slot #0, and the front cartridge slot becomes slot #1.
- That is, after the power is switched on or after the RESET switch is pushed, the CPU is started up from slot #0 0000H address, resulting in the MSX-BASIC ROM being selected and taking control of operations.
- If the ROM, RAM, and internal I/O are normal, the initial display will appear on the screen to enable key inputs under MSX-BASIC control. If an abnormal condition exists, however, resulting in runaway status or suspended operation, it will not be possible to detect that condition while under MSX-BASIC control.
- In this case, if the inspection 2 ROM made ready when the power was switched on or the RESET switch pushed can be activated and various checks executed, the location of the abnormal condition can be determined.
- In this ass'y, slot #0 can be reverted to the front cartridge slot and slot #1 to the MSX-BASIC ROM and 32K byte RAM by removing the solder from JPC or JPA, and from JPB or JPD, thereby enabling activation of the inspection 2 ROM mounted in the front cartridge.
- JPC/JPA and JPB/JPD have been mounted on the top and bottom of the ass'y for handling working top the front, or the JPC/JPD solder when working from the bottom.

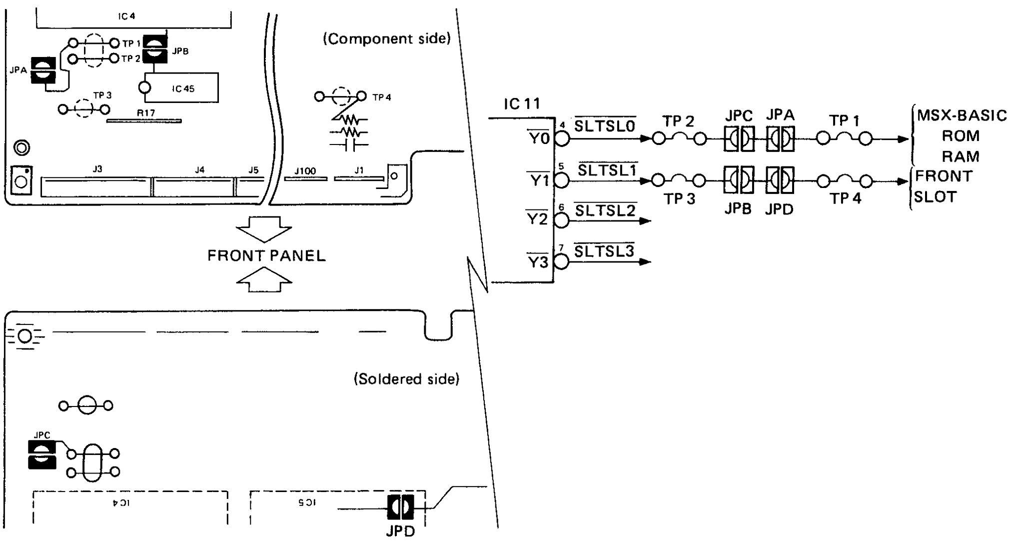


Fig. 11-7 Place and circuit diagram

11-3 INSPECTION 2

INSPECTION 2 is an 8K byte program consisting entirely of machine language, and which is activated by inserting the program in 0000H thru 1FFFH in slot #0 (in front of unit) by the slot #0/slot #1 switching described above under "CPU Ass'y TP1 Thru TP4 Functions".

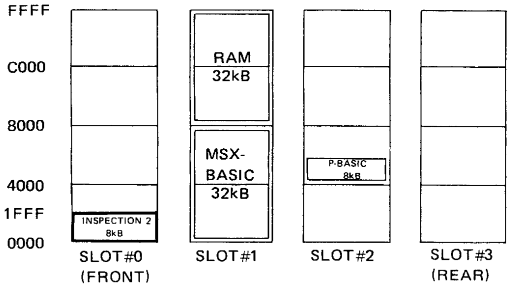


Fig. 11-8 Memory map

Connections

- Connect the RF, VIDEO, or RGB output to the display unit.
- Connect the FROM PC terminal on the CENTRONICS CHECK BOARD to the PX-7 PRINTER terminal by using MSX printer cable.
- Connect a +5V power supply by using the alligator clips connected to the TO IF terminal on the CHECK BOARD.
  * This +5V may also be supplied from the PX-7 unit.
- Switch the CENTRONICS CHECK BOARD SINGLE/CONTINUE selector to the SINGLE position.
  * SINGLE . . . . . .Test executed in single steps each time the STEP button is pressed.
  CONTINUE . . .Tests executed continuously in succession — useful in aging test.
- After first removing the bridge connecting JPA to JPB (repaired from the component side) or the bridge connecting JPC to JPD (repaired from the soldering side) connect TP1 to TP3 and TP2 to TP4 to interchange slot #0 and #1.
- Insert the INSPECTION 2 cartridge in the front panel CARTRIDGE slot.
- Adjust the VOLUME and MIXING LEVEL controls to the central positions to ensure that the sound output is at an audible level.

After completing these settings, switch the PX-7 power on to proceed with the tests listed in the Test Flow.

Test results can be checked by display, sound output, and LED lamps. Therefore, if one of the functions fails to operate, checks can still be executed by using the remaining functions.

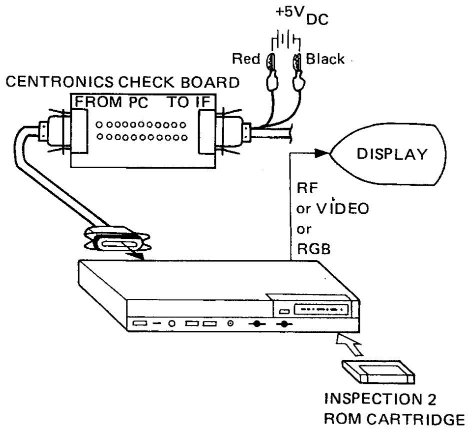


Fig. 11-9 Connections

Test Flow

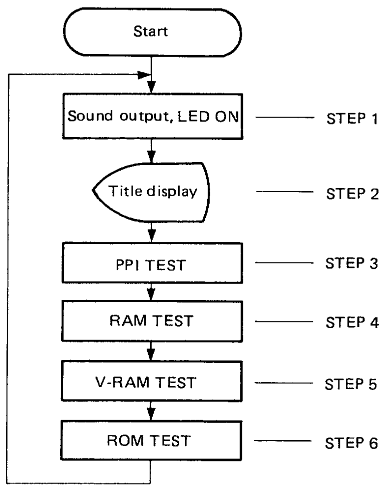


Fig. 11-10 Test flow-chart

[STEP 1] Sound Output and LED Lamps

- When the power is switched on, a continuous tone is generated by the PSG (and continues until the title is displayed).
- The D0 thru D7 LED pattern changes as shown in the accompanying diagram each time the CENTRONICS CHECK BOARD STEP button is pressed.

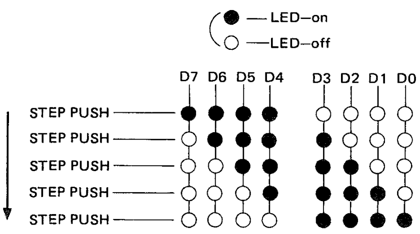


Fig. 11-11 Sound output and LED lamps

[STEP 2] Title Display

- When the STEP button is pressed again after completing STEP 1, the title is displayed on the screen (see accompanying diagram), and the PSG tone is stopped.

Operation of the basic sections and the CPU, PSG, VDP, and PRINTER PORT statuses are checked by the above steps.

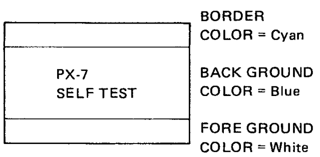


Fig. 11-12 Title display

[STEP 3] PPI Test

See fig. 11-14

[STEP 4] Ram Test

- The RAM test is executed with the RAM area divided into four parts.
  First, the area used as program work area is checked by tests ⑤ and ⑥.

Table 11-1

⑤ 8000~80FFH TEST	⑥ C000~C0FFH TEST	WORK AREA ADDRESS
OK	OK	8000~80FFH
OK	NG	8000~80FFH
NG	OK	C000~C0FFH
NG	NG	CAN'T CONTINUE

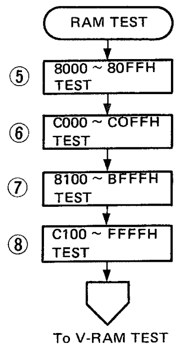
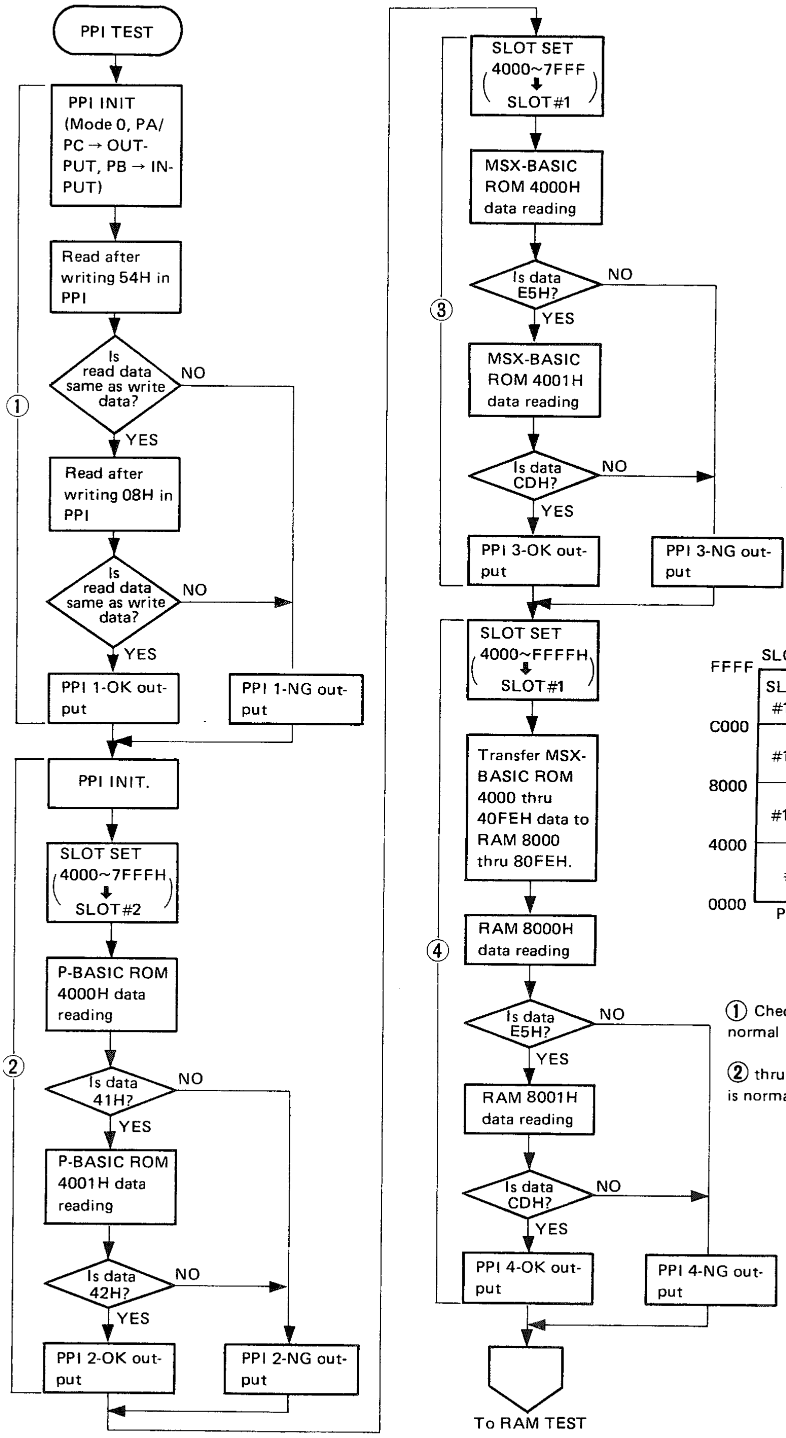


Fig. 11-13 RAM test



Address	SLOT			
FFFF–C000	SLOT #1/#0	#0	#0	#1
C000–8000	#1/#0	#0	#0	#1
8000–4000	#1/#0	#2	#1	#1
4000–0000	#0	#0	#0	#0
	PPI 1	PPI 2	PPI 3	PPI 4

Memory map changes

① Check to see that PPI accessing is normal

② thru ④ Check to see that slot setting is normal

Fig. 11-14 PPI test flow-chart

- The RAM used in the PX-7 consists of four 16K × 4-bit D-RAMs to provide 32K bytes of RAM area from 8000 to FFFFH.
- These four D-RAMs are allocated in the following way.

Table 11-2

IC15	8000 thru BFFFH	D0 thru D3
IC18	8000 thru BFFFH	D4 thru D7
IC16	C000 thru FFFFH	D0 thru D3
IC19	C000 thru FFFFH	D4 thru D7

- That is, the RAM area 8000 thru BFFFH is formed by the IC15/IC18 pair, and the C000 thru FFFFH area is formed by the IC16/IC19 pair.
- A work area can thus be secured as long as one of the above pairs is operating.
- If both pairs are NG, however, subsequent tests cannot be executed. The CAN'T CONTINUE message appears on the screen, an accompanying tone is generated, and the program is halted.

Rather than a defect in the RAM itself, NG conditions are usually due to a failure in the access stage. Therefore, when checking the circuitry, check that $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$, ADDRESS LINE, and DATA LINE are all normal.
An accessing failure will certainly be the most likely cause if the CAN'T CONTINUE condition occurs.

(WORK AREA TEST)

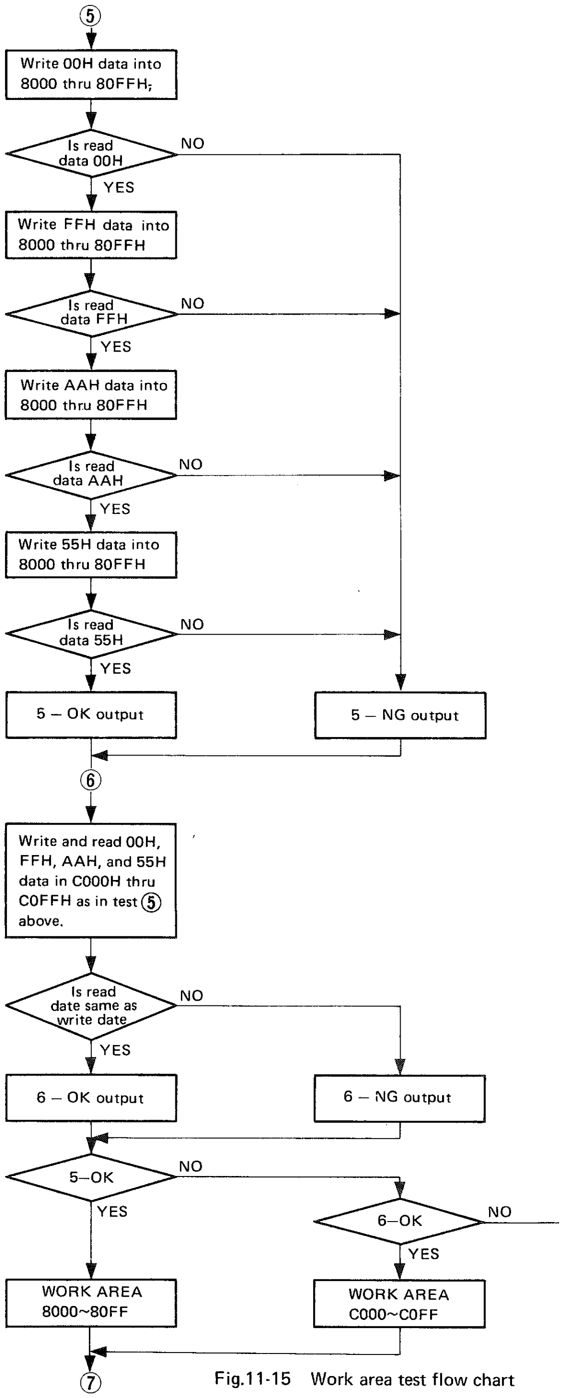


Fig.11-15 Work area test flow chart

RAM areas not checked by tests ⑤ and ⑥ are to be checked by tests ⑦ and ⑧.

- When a NG condition occurs, the NG output is accompanied by the NG address, the data read at that time, and an indicator tone.

Display examples

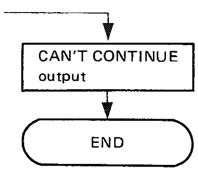
When OK

```
8100 ~ BFFF
  00 — OK
  55 — OK
  AA — OK
  FF — OK
```

When NG: 8100H is NG, resulting in reading of 7EH data.

```
8100 ~ BFFF
00 — NG 8100-7E
55 — NG 8100-7E
AA — NG 8100-7E
FF — NG 8100-7E
```

If a NG condition occurs during this test, the program proceeds to the next routine without checking the remaining addresses in NG routine. Hence, there is only a single NG address data output for any one routine.
That is, in the above NG display example, it is not possible to tell whether the remaining addresses from 8101H are OK or not.



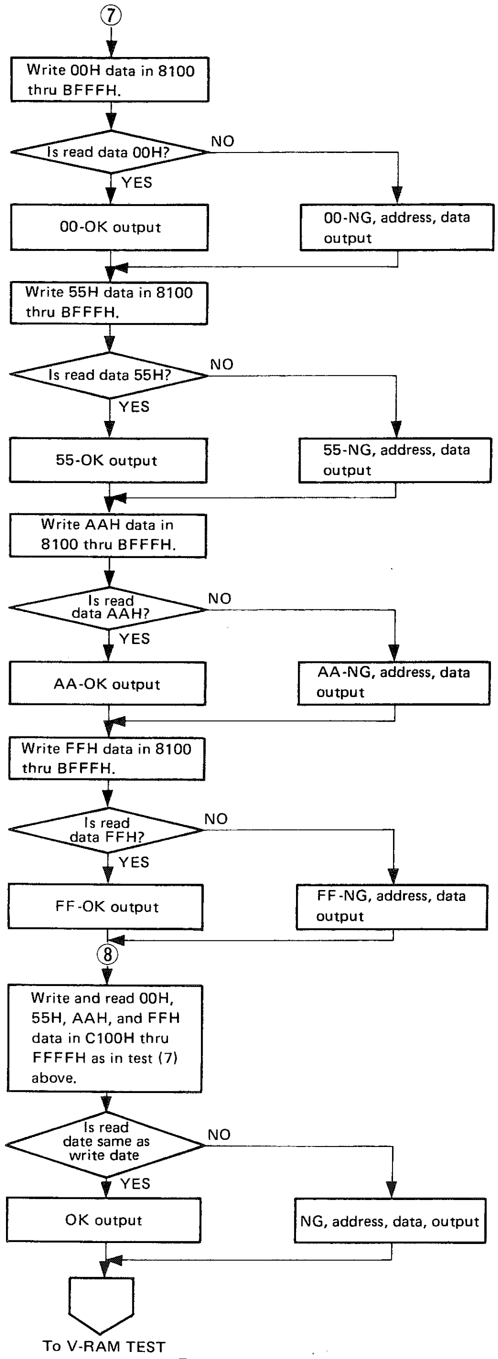


Fig. 11-16 Work area test flow chart

[STEP 5] V-RAM TEST

- The V-RAM test is executed without dividing the V-RAM address 0000H thru 3FFFH 16K byte area.
- Since the display changes during the test, the OK/NG display is not shown unitl after the check has been completed.
- If a NG output is obtained at the 55H stage of the test, the program proceeds immediately to the ROM TEST.

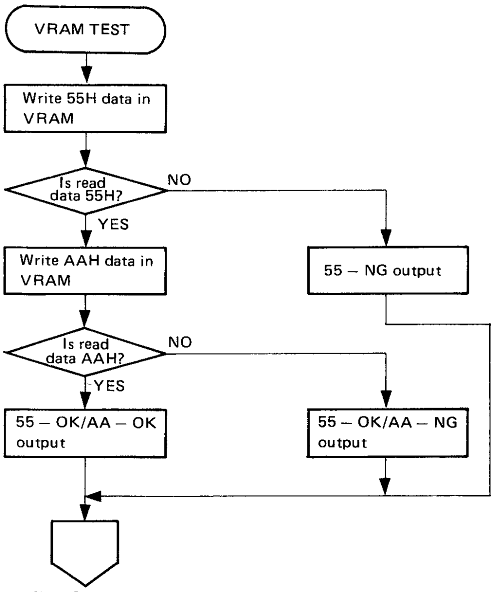


Fig. 11-17 V-RAM test flow chart

[STEP 6] Rom Test

- The ROM TEST is divided into the P-BASIC ROM TEST ⑩ and the MSX-BASIC ROM TEST ⑪ .

1. Check to see that P-BASIC ROM address 4000, 4001, 4010 thru 4012H data is as shown in the following table.

Table P-BASIC ROM address data

Address	Data (Hexadecimal)	Data (ASCII code)
4000H	41	A
4001H	42	B
4010H	50	P
4011H	4E	N
4012H	52	R

2. All P-BASIC ROM address data from 4000H to 5FFFH is summed (addition of all bytes with no carry), and a check is made to see that the sum is FFH.

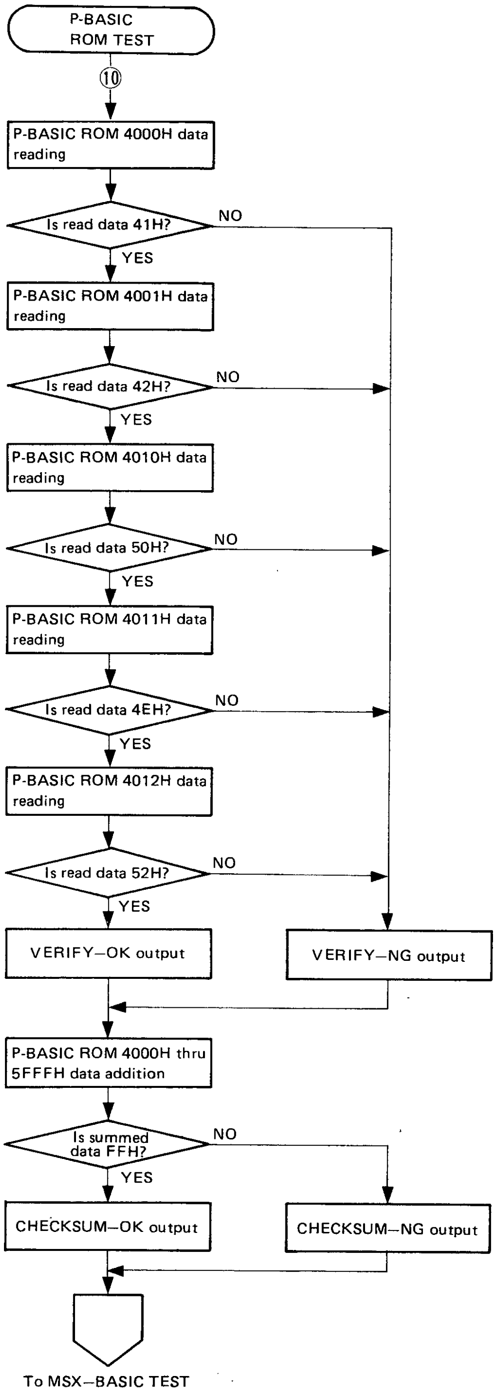
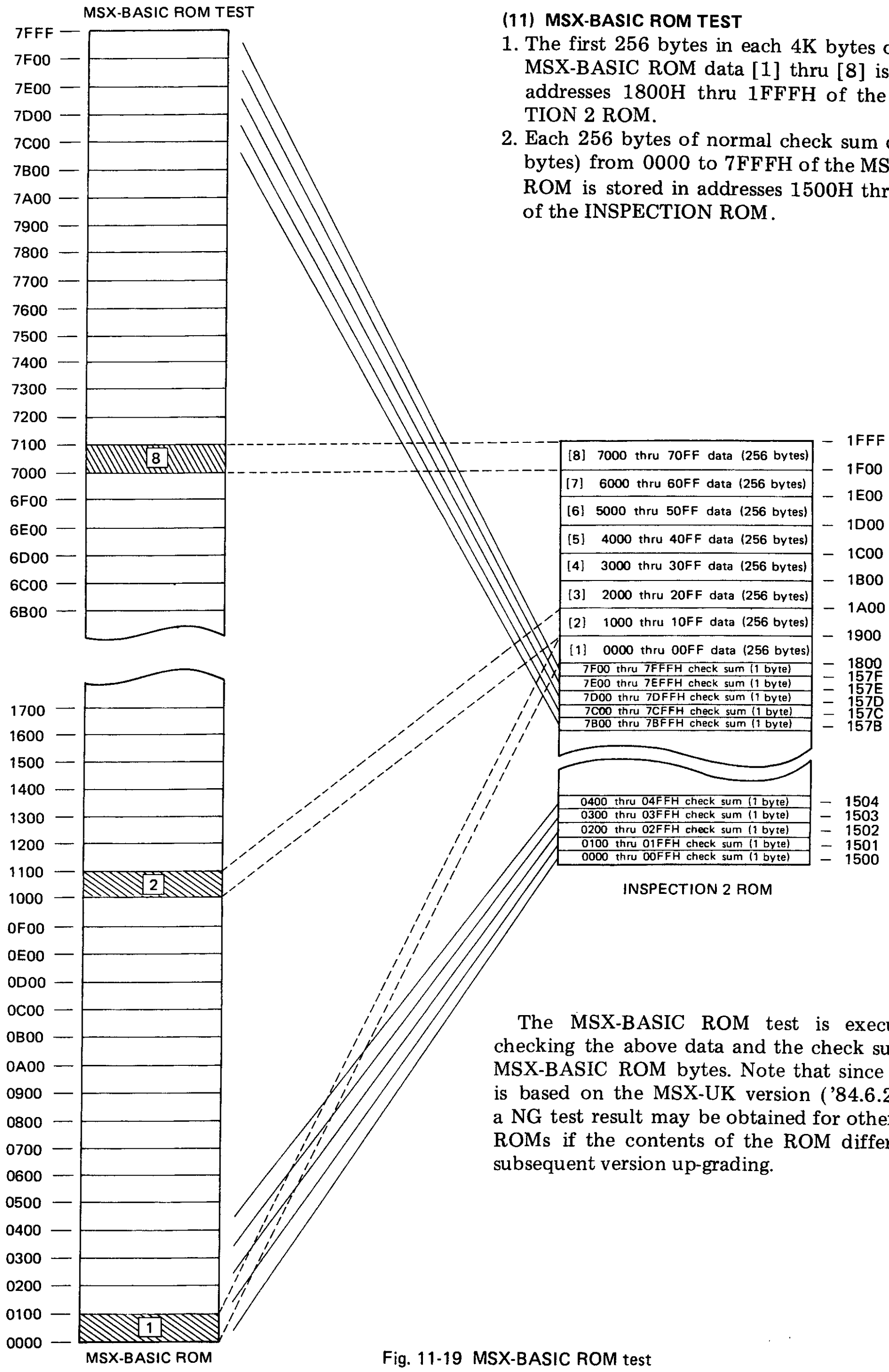


Fig. 11-18 ROM test flow-chart



(11) MSX-BASIC ROM TEST

1. The first 256 bytes in each 4K bytes of normal MSX-BASIC ROM data [1] thru [8] is stored in addresses 1800H thru 1FFFH of the INSPECTION 2 ROM.
2. Each 256 bytes of normal check sum data (128 bytes) from 0000 to 7FFFH of the MSX-BASIC ROM is stored in addresses 1500H thru 157FH of the INSPECTION ROM.

The MSX-BASIC ROM test is executed by checking the above data and the check sum of all MSX-BASIC ROM bytes. Note that since this test is based on the MSX-UK version ('84.6.29 FIX), a NG test result may be obtained for other normal ROMs if the contents of the ROM differ due to subsequent version up-grading.

Fig. 11-19 MSX-BASIC ROM test

- END is displayed on the screen when the ROM test is completed, and the program returns to the same output tone and LED pattern as in the beginning.

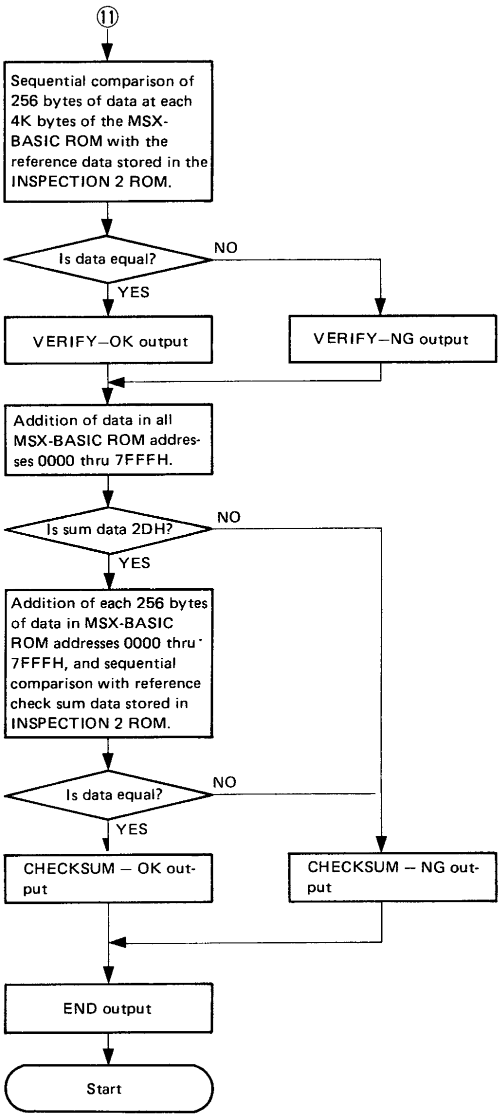


Fig. 11-20

Fig. 11-20 MSX-BASIC ROM test

Table 11-3 Inspection 2 test flow

INSPECTION 2 TEST FLOW

LED ●– On ○– Off

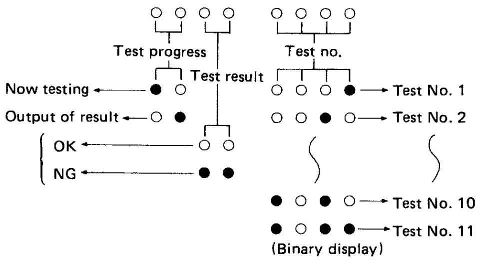
Test Description	CENTRONICS CHECK BOARD LED PATERN	D7 D6 D5 D4	D3 D2 D1 D0	DISPLAY OUT	SOUND OUT
STEP 1 Sound and LED Outputs Normal CPU, CPU peripheral circuits, gate array, and printer output can be checked by the generated tone and LED pattern changes.	STEP PUSH	● ● ● ●	○ ○ ○ ○		BEEP ON
	STEP PUSH	○ ● ● ●	● ○ ○ ○		
	STEP PUSH	○ ○ ● ●	● ● ○ ○		
	STEP PUSH	○ ○ ○ ●	● ● ● ○		
	STEP PUSH	○ ○ ○ ○	● ● ● ●		
STEP 2 Title display	STEP PUSH				
Display of title on screen, and VDP operation check				Initial screen settings Border color Cyan Background color Blue Foreground color White Title PX-7 SELF TEST	BEEP OFF
STEP 3 PPI TEST	STEP PUSH				
(1) 54H and 08H data to PPI: write, read, and verify	Now testing	*● ○ ○ ○	○ ○ ○ ●	PPI TEST 1 –	
	When result is OK	*○ ● ○ ○	○ ○ ○ ●	1 – OK	
	When result is NG	*○ ● ● ●	○ ○ ○ ●	1 – NG	BEEP
Comment	*Meaning of LED patterns  All steps described below are executed in this sequence.				Beep tone generated when result is NG
(2) Check that addresses 4000 thru 7FFFH are switched to slot #2.	STEP PUSH				
	Now testing	● ○ ○ ○	○ ○ ● ○	2 –	
	When result is OK	○ ● ○ ○	○ ○ ● ○	2 – OK	
	When result is NG	○ ● ● ●	○ ○ ● ○	2 – NG	
(3) Check that addresses 4000 thru 7FFFH are switched to slot #1.	STEP PUSH				
	Now testing	● ○ ○ ○	○ ○ ● ●	3 –	
	When result is OK	○ ● ○ ○	○ ○ ● ●	3 – OK	
	When result is NG	○ ● ● ●	○ ○ ● ●	3 – NG	BEEP
(4) Check that addresses 8000 thru BFFFH are switched to slot #1.	STEP PUSH				
	Now testing	● ○ ○ ○	○ ● ○ ○	4 –	
	When result is OK	○ ● ○ ○	○ ● ○ ○	4 – OK	
	When result is NG	○ ● ● ●	○ ● ○ ○	4 – NG	BEEP

Table 11-4 Inspection 2 test flow

Test Description	Output of Result			
	CENTRONICS CHECK BOARD	LED PATERN	DISPLAY OUT	SOUND OUT
STEP4 RAM TEST	STEP PUSH			
(5) Write, read, and verify addresses 8000 thru 80FFH	Now testing	● ○ ○ ○ ○ ● ○ ●	RAM TEST 5 –	
	When result is OK	○ ● ○ ○ ○ ● ○ ●	5 – OK	
	When result is NG	○ ● ● ● ○ ● ○ ●	5 – NG	BEEP
(6) Write, read, and verify addresses C000 thru C0FFH	STEP PUSH			
	Now testing	● ○ ○ ○ ○ ● ● ○	6 –	
	When result is OK	○ ● ○ ○ ○ ● ● ○	6 – OK	
	When result is NG	○ ● ● ● ○ ● ● ○	6 – NG	BEEP
	When result is NG in both tests (5) and (6)		CAN'T CONTINUE	Continuous beep tone
(7) Write, read, and verify addresses 8100 thru BFFFH	STEP PUSH			
	Now testing	● ○ ○ ○ ○ ● ● ●	8100H~BFFFH.	
	When result is OK	○ ● ○ ○ ○ ● ● ● (Write data) →	00 – OK 55 – OK (NG address) AA – OK (Read data) FF – OK	
	When result is NG	○ ● ● ● ○ ● ● ●	00 – NG 8100-7E 55 – NG 8100-7E AA – NG 8100-7E FF – NG 8100-7E	BEEP BEEP BEEP BEEP
(8) Write, read, and verify addresses C100 thru FFFFH	STEP PUSH			
	Now testing	● ○ ○ ○ ● ○ ○ ○	C100H~FFFFH	
	When result is OK	○ ● ○ ○ ● ○ ○ ○	00 – OK 55 – OK AA – OK FF – OK	
	When result is NG	○ ● ● ● ● ○ ○ ○	00 – NG C100 – 7E 55 – NG C100 – 7E AA – NG C100 – 7E FF – NG C100 – 7E	BEEP BEEP BEEP BEEP
STEP5 V-RAM TEST	STEP PUSH			
(9) Write, read, and verify V-RAM addresses 0000 thru 3FFFH	Now testing	● ○ ○ ○ ● ○ ○ ●	Change in screen display	
	When result is OK	○ ● ○ ○ ● ○ ○ ●	VRAM 55 – OK AA – OK	
	When result is NG	○ ● ● ● ● ○ ○ ●	VRAM 55 – NG	BEEP
STEP6 ROM TEST	STEP PUSH			
(10) Verify P-BASIC ROM data check sum	Now testing	● ○ ○ ○ ● ○ ● ○	ROM TEST P-BASIC	
	When result is OK	○ ● ○ ○ ● ○ ● ○	VERIFY – OK CHECKSUM – OK	
	When result is NG	○ ● ● ● ● ○ ● ○	VERIFY – NG CHECKSUM – NG	BEEP BEEP
(11) Verify MSX-BASIC ROM data check sum	STEP PUSH			
	Now testing	● ○ ○ ○ ○ ○ ○ ○	P-BASIC	
	When result is OK	○ ● ○ ○ ● ○ ● ●	VERIFY – OK CHECKSUM – OK	
	When result is NG	○ ● ● ● ● ○ ● ●	VERIFY – NG CHECKSUM – NG	BEEP BEEP
END			END	

Press STEP button to return to STEP 1.

Countermeasures to be Taken for Different Test Results (Analysis of Defective Positions)

Step 1 & Step 2

These tests are used to check whether test result outputs are normal or not. This program employs three means of handling test result outputs — CENTRONICS CHECK BOARD LED lamps, DISPLAY OUT, and SOUND OUT. The following tests can be executed as long as any one of these means is functioning normally. If all three are malfunctioning, however, no further testing is possible. All three means should be functioning correctly at all times.

The likely defective positions if a failure occurs are described below.

1. CENTRONICS CHECK BOARD LED → Printer interface NG
   - ○ ALL LEDs NG
     - ● Check signal between gate array (IC3) and CPU (IC1)
     - ● Check gate array (IC3) LPTE, $\overline{\text{PSTB}}$, and $\overline{\text{BUSYEN}}$ signals
     - ● Check data latch (IC32)
     - ● Check printer connector
   - ○ Some of the LEDs NG → PD0 thru PD7 NG
     - ● Check D0 thru D7, IC32, and connector
   - ○ STEP button malfunction → BUSY system NG
     - ● Check CONNECTOR (11 pin), IC45, and D1

     Subsequent tests cannot be executed if STEP button fails to function.

2. DISPLAY OUT → VDP section, analog ass'y video system NG
   - ○ No output of VDP (IC2) Y, R-Y, B-Y
     - ● Check VDP CLK
     - ● Check signal between VDP and CPU, and also check the gate array $\overline{\text{VDP}}$ signal
   - ○ Y, R-Y, and B-Y are OK, but no picture
     - ● Check analog ass'y video system
     - ● Use RGB OUT if available
   - ○ Picture obtained, but is not normal
     - ● Check signal between VDP and VRAM (IC20 & IC21)

3. SOUND OUT → PSG section analog ass'y audio system NG
   - ○ No PSG (IC5) A, B, and C outputs
     - ● Check signal between PSG and CPU
     - ● Check gate array $\overline{\text{PSG}}$ signal
     - ● Check clock input
   - ○ A, B, and C obtained, but no sound
     - ● Check ASCL and ASCR, and check Q10/Q11 if NG
     - ● Check the analog ass'y audio system

4. LEDs, DISPLAY, and SOUND all NG
   - ● Have slots #0 and #1 been switched?
   - ● Is the CPU clock (Φ) OK?
   - ● Is address bus A0 thru A15 normal?
   - ● Is data bus D0 thru D7 normal?

     Check signal matching between buffer input and output, and check short/open
   - ● Are control signals normal?
   - ● Is the front cartridege slot connector signal normal?

Step 3

PPI1 — NG (which means 2 thru 4 are also NG)
- ● Check signal between PPI (IC4) and CPU
- ● Check GATE ARRAY, $\overline{\text{PPIW}}$ and $\overline{\text{PPIR}}$ signals

PPI1 — OK, but 2, 3, or 4 NG
- ● Check PPI, PA0 thru PA7, IC28, and IC11

  2 — NG: Check between $\overline{\text{SLTSL2}}$ and P-BASIC ROM (IC13) and around the P-BASIC ROM

  3 — NG: Check between $\overline{\text{SLTSL1}}$ and MSX-BASIC ROM (IC12) and around the MSX-BASIC ROM

  4 — NG: Same check as "3 — NG" if failure in 3, but check between $\overline{\text{SLTSL1}}$ and RAM (IC15, IC16, IC18, and IC19), and around the RAM if 3 is OK.

Step 4

CAN'T CONTINUE
- ● Check GATE ARRAY, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{MPX}}$ signals, and also the IC14, IC17, IC34, and IC43 signals

5 — NG, 7 — NG
- ● Check IC15, IC18, and $\overline{\text{CAS2}}$

6 — NG, 8 — NG
- ● Check IC16, IC19, and $\overline{\text{CAS3}}$

If 5 is OK but 7 NG, or if 6 is OK but 8 NG etc, a defective RAM is the likely cause.

If the higher order bits are abnormal due to change in read data when NG, check IC18 and IC19, or if the lower order bits are abnormal, check IC15 and IC17.

Step 5

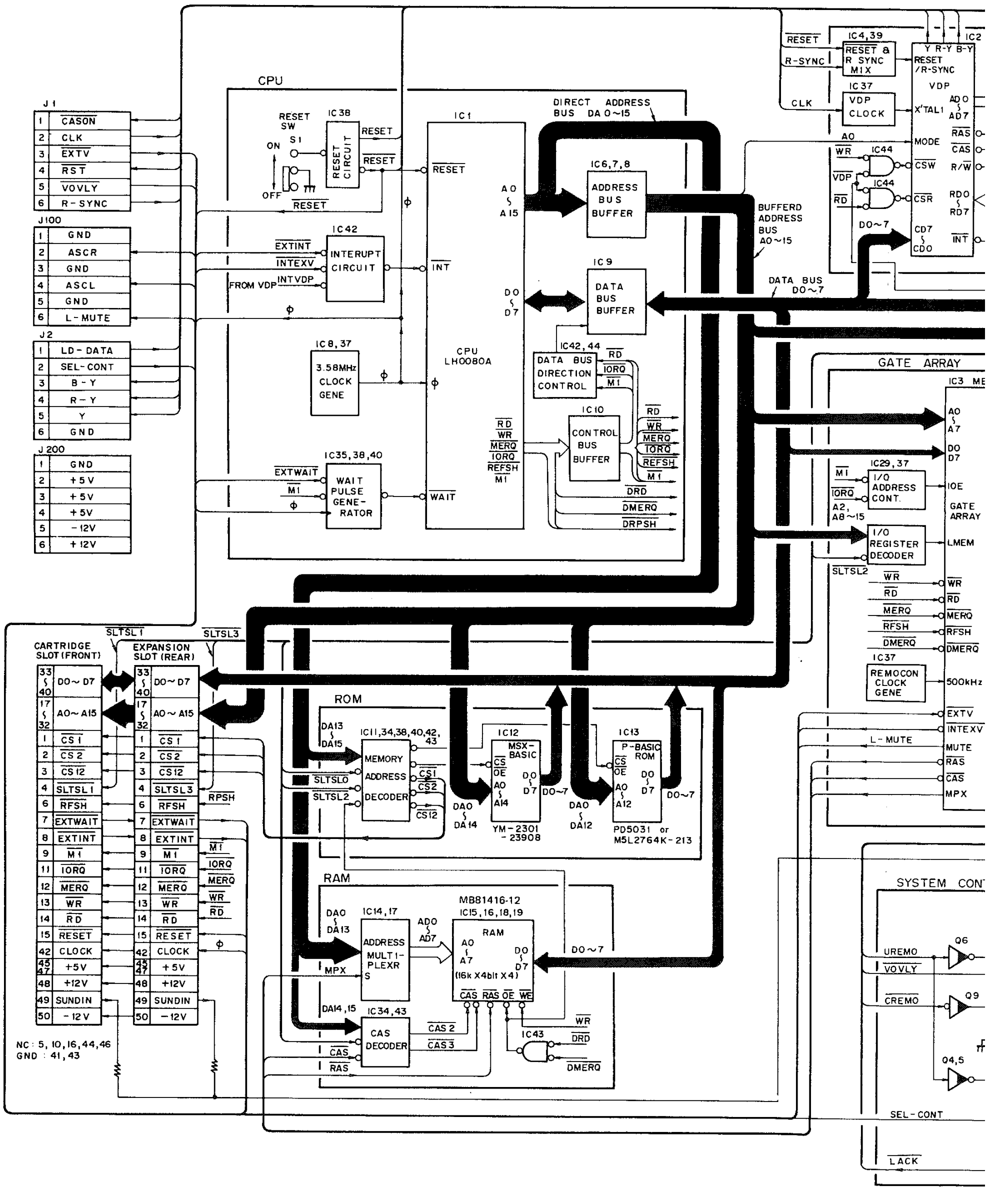
- ● Check signal between VDP and VRAM (IC20 and IC21)

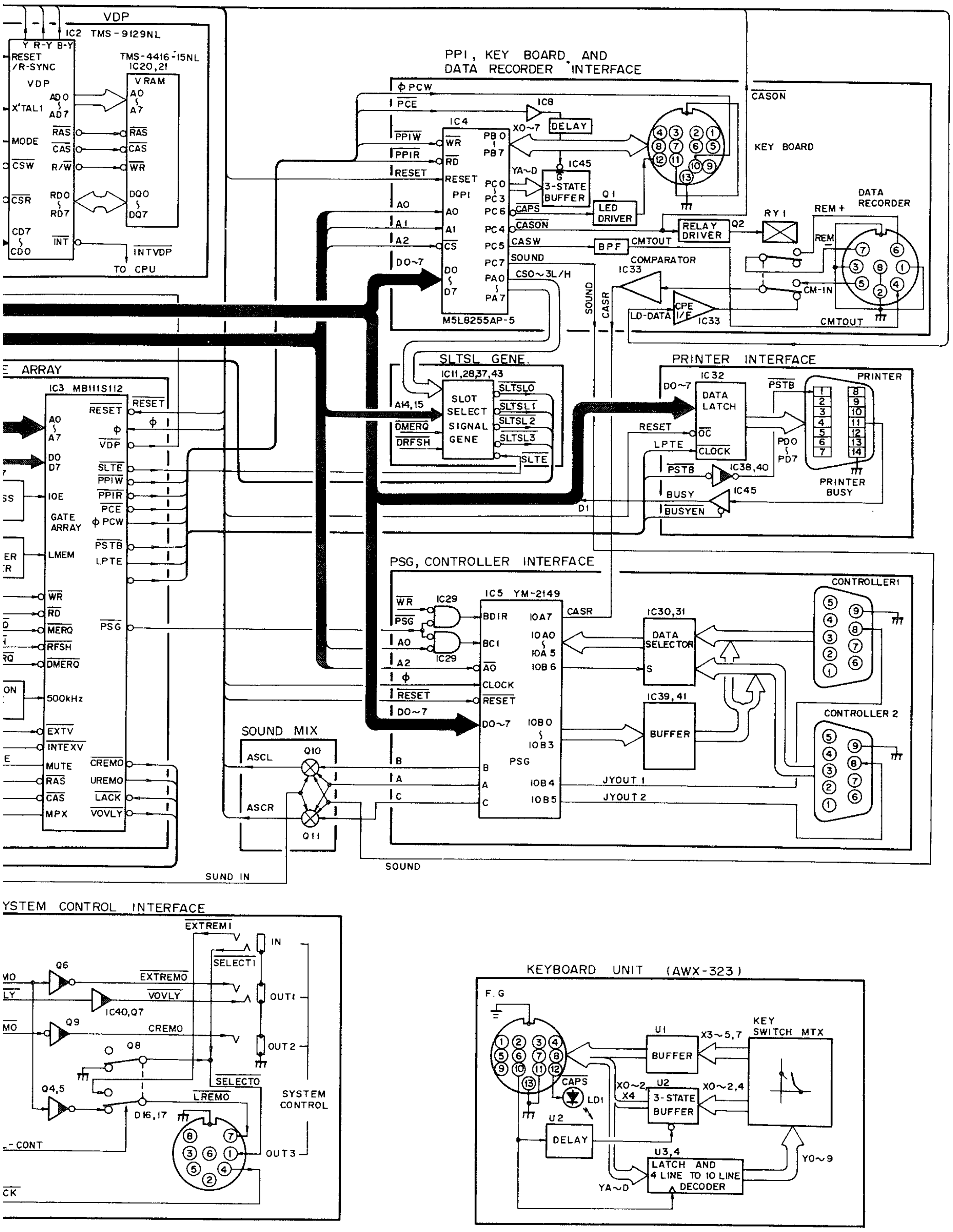
Step 6

10 — NG
- ● STEP 3 Is PPI2 OK? See STEP 3 if NG, and check P-BASIC ROM if OK

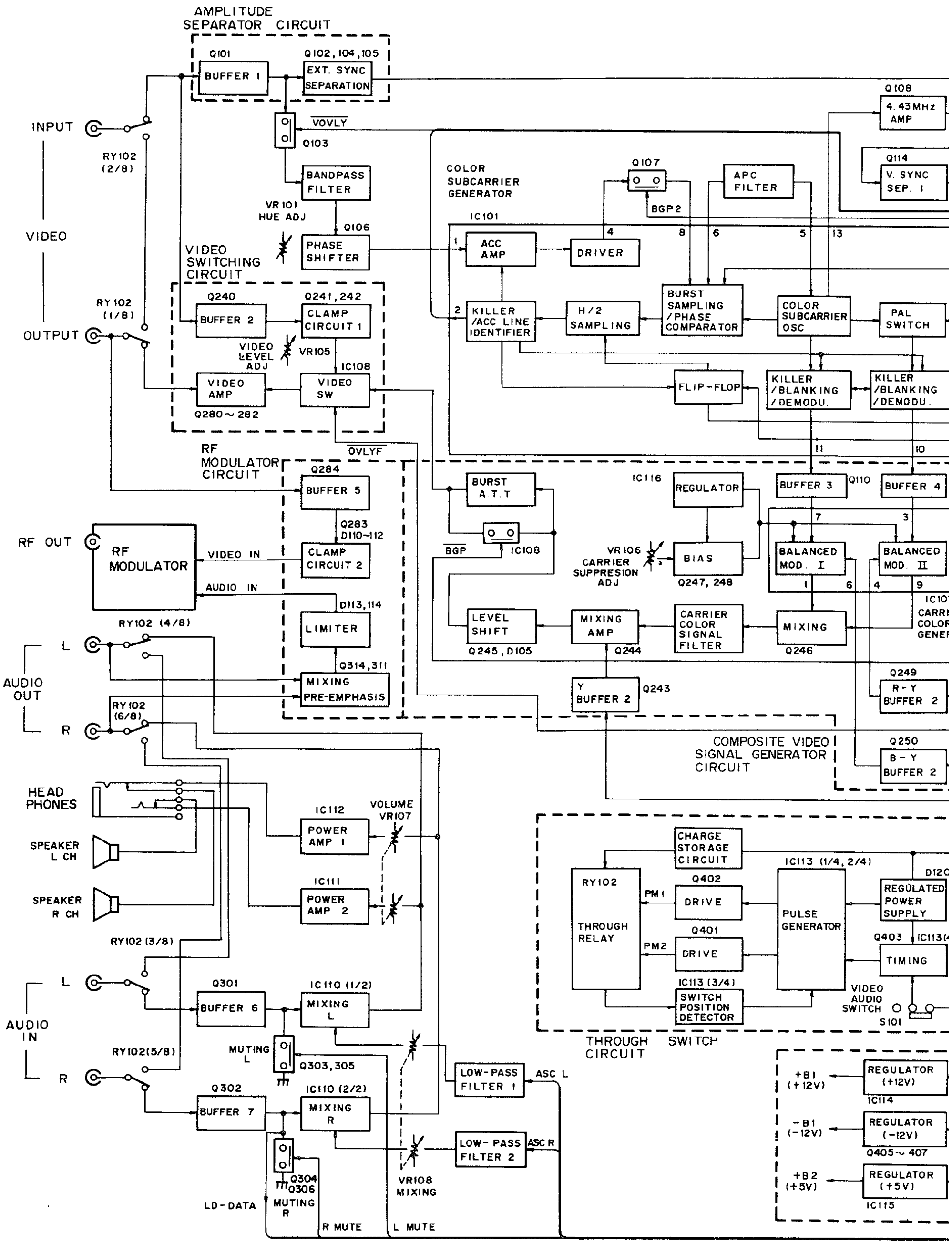
11 — NG
- ● STEP 3 Is PPI3 OK? See STEP 3 if NG, and check MSX-BASIC ROM if OK

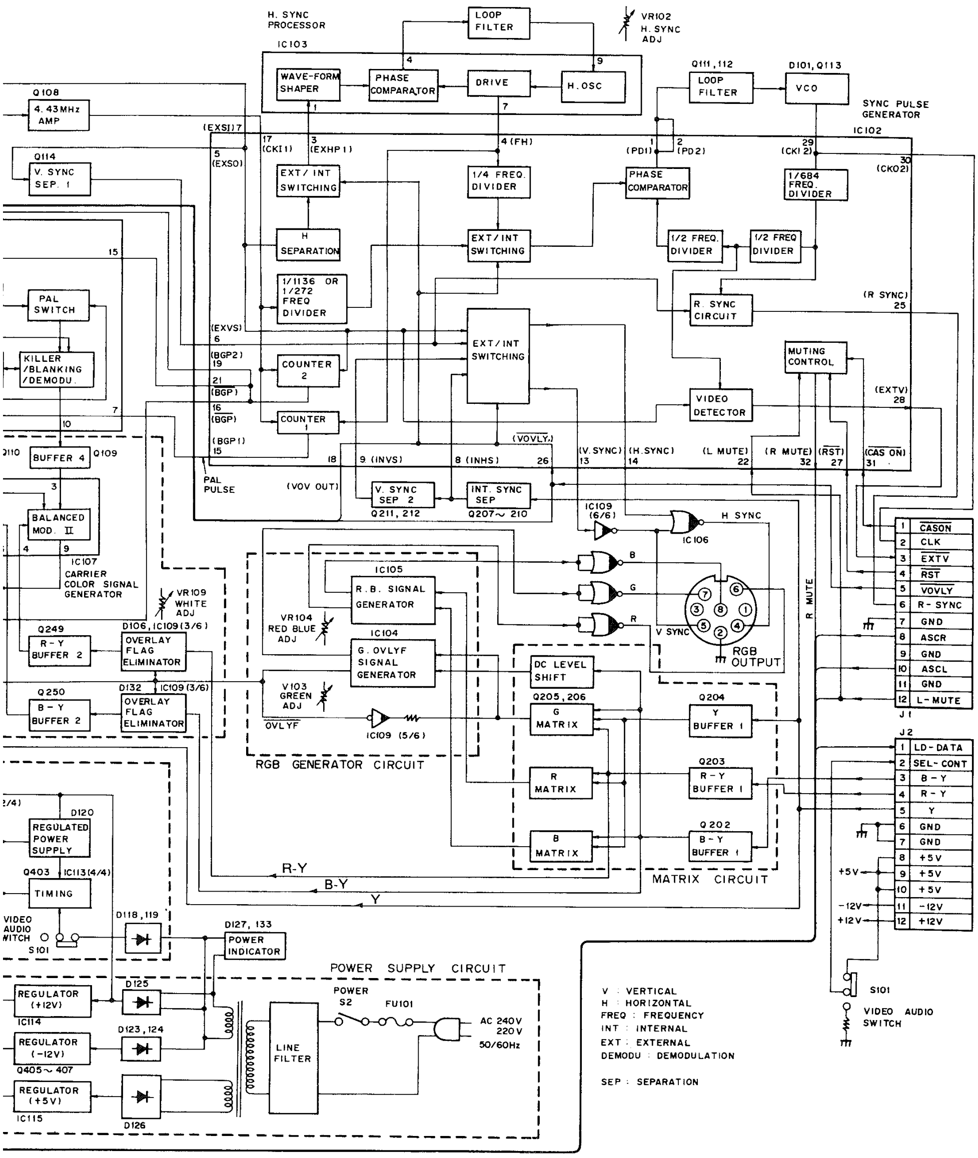
12. BLOCK DIAGRAM





VDP
IC2 TMS-9129NL
TMS-4416-15NL
IC20,21
VRAM
PPI, KEY BOARD, AND DATA RECORDER INTERFACE
IC4
PPI
M5L8255AP-5
IC8
DELAY
IC45
3-STATE BUFFER
Q1
LED DRIVER
KEY BOARD
CASON
RELAY DRIVER
Q2
RY1
REM+
DATA RECORDER
BPF
CMTOUT
COMPARATOR
IC33
LD-DATA
CPE I/F
CM-IN
SOUND
CASR
E ARRAY
IC3 MB111S112
GATE ARRAY
SLTSL GENE.
IC11,28,37,43
SLOT SELECT SIGNAL GENE
PRINTER INTERFACE
IC32
DATA LATCH
PRINTER
IC38,40
PRINTER BUSY
PSG, CONTROLLER INTERFACE
IC29
IC5 YM-2149
PSG
IC30,31
DATA SELECTOR
IC39,41
BUFFER
CONTROLLER1
CONTROLLER 2
JYOUT 1
JYOUT 2
SOUND MIX
ASCL
ASCR
Q10
Q11
SUND IN
SOUND
YSTEM CONTROL INTERFACE
EXTREM1
SELECT1
IN
OUT1
OUT2
OUT3
SELECTO
LREMO
SYSTEM CONTROL
Q6
EXTREMO
VOVLY
IC40,Q7
Q9
CREMO
Q8
Q4,5
D16,17
KEYBOARD UNIT (AWX-323)
F.G
U1
BUFFER
X3~5,7
KEY SWITCH MTX
CAPS
LD1
U2
3-STATE BUFFER
X0~2,4
DELAY
U3,4
LATCH AND 4 LINE TO 10 LINE DECODER
YA~D
Y0~9


AMPLITUDE SEPARATOR CIRCUIT
Q101
BUFFER 1
Q102, 104, 105
EXT. SYNC SEPARATION
INPUT
VIDEO
OUTPUT
RY102 (2/8)
RY102 (1/8)
Q103
VOVLY
BANDPASS FILTER
VR101 HUE ADJ
Q106
PHASE SHIFTER
VIDEO SWITCHING CIRCUIT
Q240
BUFFER 2
Q241, 242
CLAMP CIRCUIT 1
VIDEO LEVEL ADJ
VR105
IC108
VIDEO AMP
VIDEO SW
Q280～282
OVLYF
RF MODULATOR CIRCUIT
Q284
BUFFER 5
Q283
D110～112
CLAMP CIRCUIT 2
RF OUT
RF MODULATOR
VIDEO IN
AUDIO IN
D113, 114
LIMITER
Q314, 311
MIXING PRE-EMPHASIS
RY102 (4/8)
RY102 (6/8)
AUDIO OUT
HEAD PHONES
SPEAKER L CH
SPEAKER R CH
IC112
POWER AMP 1
VOLUME VR107
IC111
POWER AMP 2
RY102 (3/8)
AUDIO IN
RY102 (5/8)
Q301
BUFFER 6
IC110 (1/2)
MIXING L
MUTING L
Q303, 305
Q302
BUFFER 7
IC110 (2/2)
MIXING R
Q304
Q306
MUTING R
LD-DATA
R MUTE
L MUTE
VR108 MIXING
LOW-PASS FILTER 1
ASC L
LOW-PASS FILTER 2
ASC R
COLOR SUBCARRIER GENERATOR
IC101
Q107
BGP2
APC FILTER
Q108
4.43MHz AMP
Q114
V. SYNC SEP. 1
ACC AMP
DRIVER
KILLER /ACC LINE IDENTIFIER
H/2 SAMPLING
BURST SAMPLING /PHASE COMPARATOR
COLOR SUBCARRIER OSC
PAL SWITCH
FLIP-FLOP
KILLER /BLANKING /DEMODU.
KILLER /BLANKING /DEMODU.
IC116
BURST A.T.T
BGP
IC108
REGULATOR
BUFFER 3
Q110
BUFFER 4
VR106 CARRIER SUPPRESION ADJ
BIAS
Q247, 248
BALANCED MOD. I
BALANCED MOD. II
LEVEL SHIFT
Q245, D105
MIXING AMP
Q244
CARRIER COLOR SIGNAL FILTER
MIXING
Q246
Y BUFFER 2
Q243
Q249
R-Y BUFFER 2
COMPOSITE VIDEO SIGNAL GENERATOR CIRCUIT
Q250
B-Y BUFFER 2
CHARGE STORAGE CIRCUIT
IC113 (1/4, 2/4)
RY102
THROUGH RELAY
PM1
PM2
Q402
DRIVE
Q401
DRIVE
PULSE GENERATOR
REGULATED POWER SUPPLY
Q403
TIMING
IC113 (3/4)
SWITCH POSITION DETECTOR
VIDEO AUDIO SWITCH
S101
THROUGH SWITCH CIRCUIT
+B1 (+12V)
REGULATOR (+12V)
IC114
-B1 (-12V)
REGULATOR (-12V)
Q405～407
+B2 (+5V)
REGULATOR (+5V)
IC115



H. SYNC PROCESSOR
IC103
LOOP FILTER
VR102 H. SYNC ADJ
WAVE-FORM SHAPER
PHASE COMPARATOR
DRIVE
H. OSC
Q111, 112
LOOP FILTER
D101, Q113
VCO
SYNC PULSE GENERATOR
IC102
Q108
4.43MHz AMP
Q114
V. SYNC SEP. 1
EXT/INT SWITCHING
1/4 FREQ. DIVIDER
PHASE COMPARATOR
1/684 FREQ. DIVIDER
H SEPARATION
EXT/INT SWITCHING
1/2 FREQ. DIVIDER
1/2 FREQ DIVIDER
1/1136 OR 1/272 FREQ DIVIDER
R SYNC CIRCUIT
PAL SWITCH
EXT/INT SWITCHING
MUTING CONTROL
KILLER /BLANKING /DEMODU.
COUNTER 2
COUNTER 1
VIDEO DETECTOR
BUFFER 4
Q109
PAL PULSE
V. SYNC SEP 2
Q211, 212
INT. SYNC SEP
Q207~210
BALANCED MOD. II
IC107 CARRIER COLOR SIGNAL GENERATOR
IC109 (6/6)
IC106
H SYNC
IC105
R.B. SIGNAL GENERATOR
VR104 RED BLUE ADJ
IC104
G. OVLYF SIGNAL GENERATOR
V103 GREEN ADJ
OVLYF
IC109 (5/6)
RGB GENERATOR CIRCUIT
VR109 WHITE ADJ
Q249
R-Y BUFFER 2
D106, IC109(3/6)
OVERLAY FLAG ELIMINATOR
Q250
B-Y BUFFER 2
D132 IC109(3/6)
OVERLAY FLAG ELIMINATOR
V SYNC
RGB OUTPUT
R MUTE
DC LEVEL SHIFT
Q205, 206
G MATRIX
R MATRIX
B MATRIX
Q204
Y BUFFER 1
Q203
R-Y BUFFER 1
Q202
B-Y BUFFER 1
MATRIX CIRCUIT
R-Y
B-Y
Y
D120
REGULATED POWER SUPPLY
Q403 IC113(4/4)
TIMING
VIDEO AUDIO SWITCH
S101
D118, 119
D127, 133
POWER INDICATOR
POWER SUPPLY CIRCUIT
REGULATOR (+12V)
IC114
D125
REGULATOR (-12V)
Q405~407
D123, 124
REGULATOR (+5V)
IC115
D126
LINE FILTER
POWER S2
FU101
AC 240V 220V 50/60Hz
J1
1 CASON
2 CLK
3 EXTV
4 RST
5 VOVLY
6 R-SYNC
7 GND
8 ASCR
9 GND
10 ASCL
11 GND
12 L-MUTE
J2
1 LD-DATA
2 SEL-CONT
3 B-Y
4 R-Y
5 Y
6 GND
7 GND
8 +5V
9 +5V
10 +5V
11 -12V
12 +12V
S101
VIDEO AUDIO SWITCH
V : VERTICAL
H : HORIZONTAL
FREQ : FREQUENCY
INT : INTERNAL
EXT : EXTERNAL
DEMODU : DEMODULATION
SEP : SEPARATION

13. CIRCUIT DESCRIPTION

13. 1 BLOCK DIAGRAM DESCRIPTION

● TOTAL, CPU

1. CPU (Central Processing Unit)

- LH0080A (Z80A equivalent) (3.58MHz clock frequency)
- 1 WAIT generated during instruction fetch (M1) cycle
- Mode 0, 1, and 2 interrupt processing from $\overline{INT}$ pin possible (without using $\overline{NMI}$)
  Interrupts include
  1) Interrupt for each single feed scan from VDP (50Hz cycle)
  2) Interrupt when external video signal is switched off in superimpose or video mode
  3) Interrupt from external device via cartridge slot

2. ROM (Read Only Memory)

- 32K bytes masking ROM (YM-2301-23908 used as built-in MSX-BASIC interpreter (UK version)
- 8K bytes masking ROM (PD5031) used as built-in extension P-BASIC interpreter ROM. Substitute EP-ROM (M5L2764K-213)
- Total ROM area of 40K bytes

3. RAM (Random Access Memory)

- 32K bytes RAM
- Four 16K × 4-bit D-RAMs (MB81416-12 or M5M4416P-15) used as RAM

4. VDP, V-RAM, and RF MOD

- TMS9129NL (PAL system color difference signal output). 16K bytes V-RAM
- Two 16K × 4-bit D-RAMs (TMS4416-15NL or M5M4416p-15) used as V-RAM
- 256 × 192 dots 16 color display (including transparent, black, and white). 32 sprites (dynamic picture) pattern generation possible

5. Video Circuit and Interface

- RGB (TTL level digital output) and PAL composite output and RF output are generated from VDP color difference output, and combination with external composite input signal (three modes: superimpose, video, and computer)

6. PPI (Programmable Peripheral Interface)

- M5L8255AP-5 with three built-in 8-bit I/O ports (PA0 thru PA7, PB0 thru PB7, PC0 thru PC7)
- Mode A used with PA0 thru PA7 set as output, PB0 thru PB7 set to input, and PC0 thru PC7 set to output
- PA0 thru PA7 allocated to slot selection, PB0 thru PB7, PC0 thru PC3 and PC6 to keyboard I/F, PB4 and PB5 to data recorder I/F, and PC7 to sound output

7. Keyboard Interface

- Output of scan signals to keyboard key matrix, and input of key input (return) signal
- Number of connector cable lines reduced by transferring scan output and key input signals via bidirectional bus

8. PSG (Programmable Sound Generator)

- YM-2149 with three sound output channels A, B, and C (8 octave and 1 noise output) and two 8-bit I/O ports (IOA0 thru IOA7 and IOB0 thru IOB7)
- IOA0 thru IOA7 used as input ports and IOB0 thru IOB7 used as output ports
- IOA0 thru IOA5 and IOB0 thru IOB6 are used as control 1 and 2 I/Fs, and IOA7 is used as data recorder data input
- Other ports are not used

9. Audio Data Interface

- Data recorder data input/output and motor control

10. CPE Disk Interface

- Conversion of right channel audio data signal from CPE (Computer Program Encoded) disc to TTL levels

11. Muting Control, Sound Mixer, and Interface

- Allocation and mixing of PSG outputs A (center), B (left channel), C (right channel), PPI SOUND output (center), and cartridge slot SUNDIN input (center), and removal of unwanted harmonic components by LPF.
  External audio inputs (with independent left and right muting on/off switching by muting control) plus mixed audio and speaker outputs are also obtained.

12. System Control Interface

- PIONEER's standard remote control devices and LD-1100 remote control interface

13. Printer Interface

- 8-bit parallel printer interface in conformity with CENTRONICS specifications

14. Cartridge Slots #1 (Front) and #3 (Rear)

- Connector for MSX cartridge — input/output of MSX signals via 50-pin cartridge connector

15. Power Supply

- +5V, +12V, and −12V regulated voltages from 220/240V AC 50/60Hz input
- Current limiting of regulated outputs to protect cartridge from destruction by incorrect shorting in a slot

• ANALOG ASS'Y

A. Video Signal Circuits

1. Buffer 1

Buffer amplifier for external video signals applied via the video input terminal.

2. External Synchronizing Signal Separator

Separation of the vertical and horizontal synchronizing signals as a composite synchronizing signal from the external video signal.

3. Internal Synchronizing Signal Separator

Separation of the vertical and horizontal synchronizing signals as a composite synchronizing signal from the VDP (TMS9129) Y (luminance) signal.

4. Vertical Synchronizing Signal Separator Circuits 1 & 2

Separation of the vertical synchronizing signal from the composite synchronizing signal separated from the external video and VDP Y signals.

5. Bandpass Filter

Extraction of the chroma signal from the external video signal. (The chroma signal is muted by Q103 when in computer picture mode.)

6. Phase Shifter

Adjustment of the burst phase of the external video signal at the video switching circuit to match the computer picture color phase reference.

7. Color Subcarrier Generator Circuit

The color subcarrier generator circuit consists of a quartz resonator PLL circuit, and in superimpose mode, it is used to form a continuous color subcarrier by synchronizing with the color synchronizing signal (color burst) in the external video signal. The color subcarrier (4.433618 MHz) is used as the carrier (two signals 90° out of phase with each other) for the carrier color signal modulator.

In computer picture mode, PLL operation is stopped and the color subcarrier frequency becomes the free-running frequency. This carrier is also used as the reference clock for the synchronizing pulse generator.

8. Horizontal Synchronizing Signal Processing Circuit

The horizontal synchronizing signal processing circuit consists of a PLL circuit to form a pulse (15.625kHz) signal synchronized with the horizontal synchronizing signal in the external video signal when in superimpose mode. This pulse signal serves as the reference signal for the VDP clock (10.6MHz) generator. The horizontal synchronization adjustment control (VR102) is used to adjust the free-running frequency, and is capable of a certain degree of horizontal position adjustment if within the PLL circuit lock range. This pulse signal is also used as the PAL pulse for control of the PAL switch in the color subcarrier generator circuit in both computer and superimpose modes.

9. Loop Filter and VCO

This circuit consists of a PLL circuit together with the frequency divider and phase comparator in the synchronizing pulse generator which forms part of the 10.6MHz VDP clock generator for the CPU ass'y.

10. Synchronizing Pulse Generator

The synchronizing pulse generator consists of the following blocks.

(1) Horizontal synchronizing signal noise suppressor
(2) External video signal detector
(3) 10.6MHz PLL generator phase comparator and frequency divider
(4) Reference signal generator of 10.6MHz PLL generator.
(5) Reference signal switching circuit for the PLL generator and horizontal and vertical synchronizing signals used in superimpose.
(6) Counter 1 for PAL pulse generation
(7) Counter 2 for generation of the burst gate pulse from the external/internal horizontal synchronizing signals

(8) R.SYNC circuit for generation of VDP horizontal and vertical counter reset pulses in picture superimpose mode
(9) Muting control circuit for muting of the audio right channel

11. Matrix Circuit

The matrix circuit contains the following blocks.
(1) Y, R-Y, B-Y, buffer 1
Buffer amplifier for the computer video outputs Y (luminance signal), R-Y, and B-Y (color difference signal) from the VDP (CPU ass'y TMS9129).
(2) R, G, and B Matrix Circuits
Adder circuit to obtain the R, G, and B signals from the VDP Y, R-Y, and B-Y signals.
The R signal is generated from the R-Y and Y signals (R matrix)
The G signal is generated from the R-Y, B-Y and Y signals (G matrix)
The B signal is generated from the B-Y and Y signals (B matrix)
(3) DC level shift circuit
The VDP B-Y signal is subject to a voltage shift to enable detection of picture overlay flags in that signal.

12. RGB Generator

The RGB generator consists of the following blocks.
(1) R.B. signal generator
The R.B. signal generated in the matrix circuit is coverted to the R.B. signal of the digital R.G.B signal by voltage comparator. The R.B adjustment control (VR 104) is made up of the comparator slice adjustment volume.
(2) G.OVLYF signal generator
The G signal generated in the matrix circuit and the level-shifted B-Y signal are converted to the G and OF (picture overlay flag) signals of the digital R.G.B signal by voltage comparator.

13. Composite Video Signal Generator

This circuit consists of the following blocks.
(1) Buffer 3 and buffer 4
Optimization of the level of the color subcarrier applied to the carrier color signal modulator.
The carrier phase is inverted in buffer 3 to correct the polarity of the carrier color signal in the carrier color signal modulator.
(2) Carrier color signal modulator, voltage regulator, and bias circuit.
The carrier color signal is generated by modulating the VDP R-Y and B-Y signals to the color subcarrier (4.433618MHz). The color subcarrier suppression adjustment control (VR106) is made up of the bias adjustment volume of the carrier color signal modulator. And the voltage regulator supplies power for the carrier color signal modulator bias circuit.
(3) Mixing circuit and carrier color signal filter
The R-Y and B-Y carrier color signals generated in the color signal modulator are combined by a mixing circuit. Dot interference is reduced by restricting the carrier color signal side bands by bandpass filter.
(4) Mixing circuit and Y buffer 2
The VDP Y signal is passed through Y buffer 2 where it is combined with the carrier color signal to form the composite video signal.
(5) Level shift circuit
The level of the internal video signal is shifted to match the level of the external video signal.
(6) Burst attenuator
The burst period of the internal video signal During IC108 is opened while in computer mode to attenuate the burst signal to the standard PAL system burst level.
(7) Overlay flag eliminator
During picture superimpose mode, the overlay flag included in the VDP R-Y and B-Y color difference signals are in blank during that interval to obtain an achromatic color difference level. The white level adjustment control (VR109) is used in this level setting.
(8) R-Y and B-Y buffer 2
Buffer amplifier for the color difference signal after level compensation at the overlay flag eliminator.

14. Video Switching Circuit

The video switching circuit contains the following blocks.
(1) Buffer 2 and clamp circuit 1
The pedestal level of the external video signal is exactly matched with the pedestal level of the internal video signal. The video level adjustment control (VR105) is used in this level setting.
(2) Video switching circuit
In computer mode, external video signal mode, and picture superimpose mode, the video signal is switched by the $\overline{\text{OVLYF}}$ signal (picture superimpose flag).
(3) Video amplifier
Amplification of the video switching circuit output video signal to 1Vp-p/75 ohms.

15. RF Modulator

The RF modulator includes the following blocks.

(1) Buffer 5 and clamp circuit 2
The RF modulator modulation ratio is optimized to ensure that the synchronization destination voltage of the video signal from the video output terminals is kept at 0V.

(2) Mixing/pre-emphasis circuit
Conversion of audio left and right channel outputs to monaural by mixing circuit, and performing pre emphasis by emphasizing the high frequency components.

(3) Limiter
The audio output level is limited to prevent over modulation of the RF modulator.

B. Audio Signal Circuits

1. Buffer 6 and Buffer 7

Buffer amplifier for conversion of the audio input impedance.

2. Low-pass Filters 1 & 2

12dB/oct low-pass filters (fo = 16kHz) for audio signals from PSG (YM-2149) and PPI (8255) in the CPU ass'y.

3. L & R Muting

External audio signal muting circuits for independent left and right channel muting.

4. L & R Mixing Circuits

Adder circuits using operational amplifiers for mixing the external audio and ASC (PSG, PPI, SOUND IN) signals.

5. Power Amplifiers 1 & 2

Amplification of the mixed left and right channel audio signals to speaker and headphone driver levels.

C. Through Switch Circuits

1. Through Relay

Switching relay for output of external video and audio signals applied to the VIDEO and AUDIO INPUT terminals direct to the VIDEO and AUDIO OUTPUT terminals (through) or input to the ass'y processing circuits (normal). The relay consists of two plungers PM1 and PM2, and relay switches RY102-(1/8) thru (8/8) in an integrated device.

2. Driver Circuit

Driver circuit used to activate the through relay plungers PM1 and PM2 to switch RY102.

3. Charge Storage Circuit

This circuit supplies the power to drive plungers PM1 and PM2.

4. Switch Position Detector

This detector circuit checks that the relay switch has been properly switched by plunger action, and feeds the result back to the pulse generator circuit.

5. Pulse Generator

Generation of pulse signals to be passed to the driver circuit to drive plunger PM1 or PM2 on the basis of information received from the timing circuit and the switch position detector.

6. Timing Circuit

This timing circuit is involved in setting the switching timing for the through switch, and passing a trigger to the pulse generator.

7. Rectifier

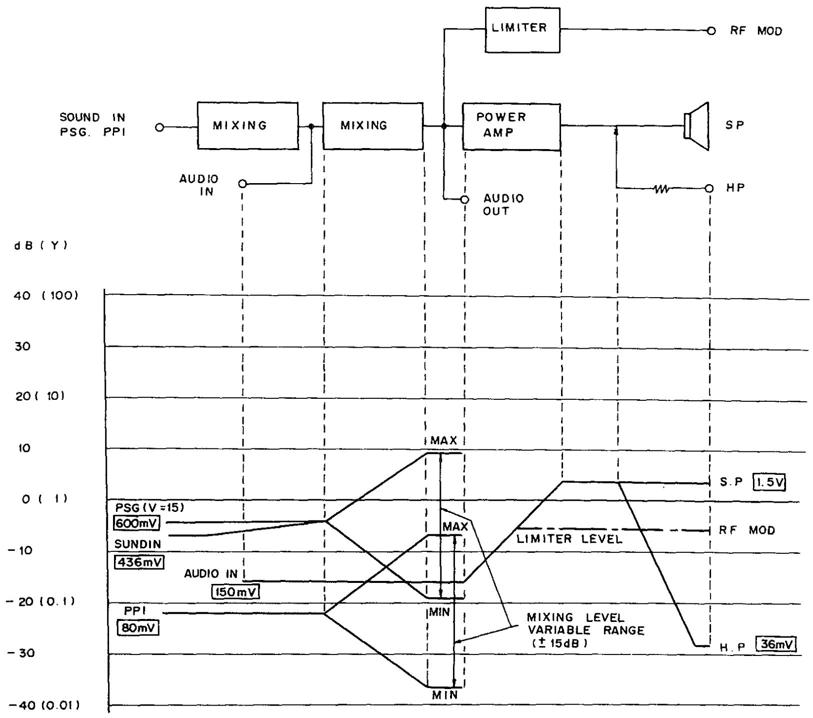
Generation of voltage for switching the timing circuit on and off.

8. Regulator

Supply of power to the timing circuit and pulse generator.

PX

- **Level Diagram**



13. 2 CPU AND PERIPHERAL CIRCUITS

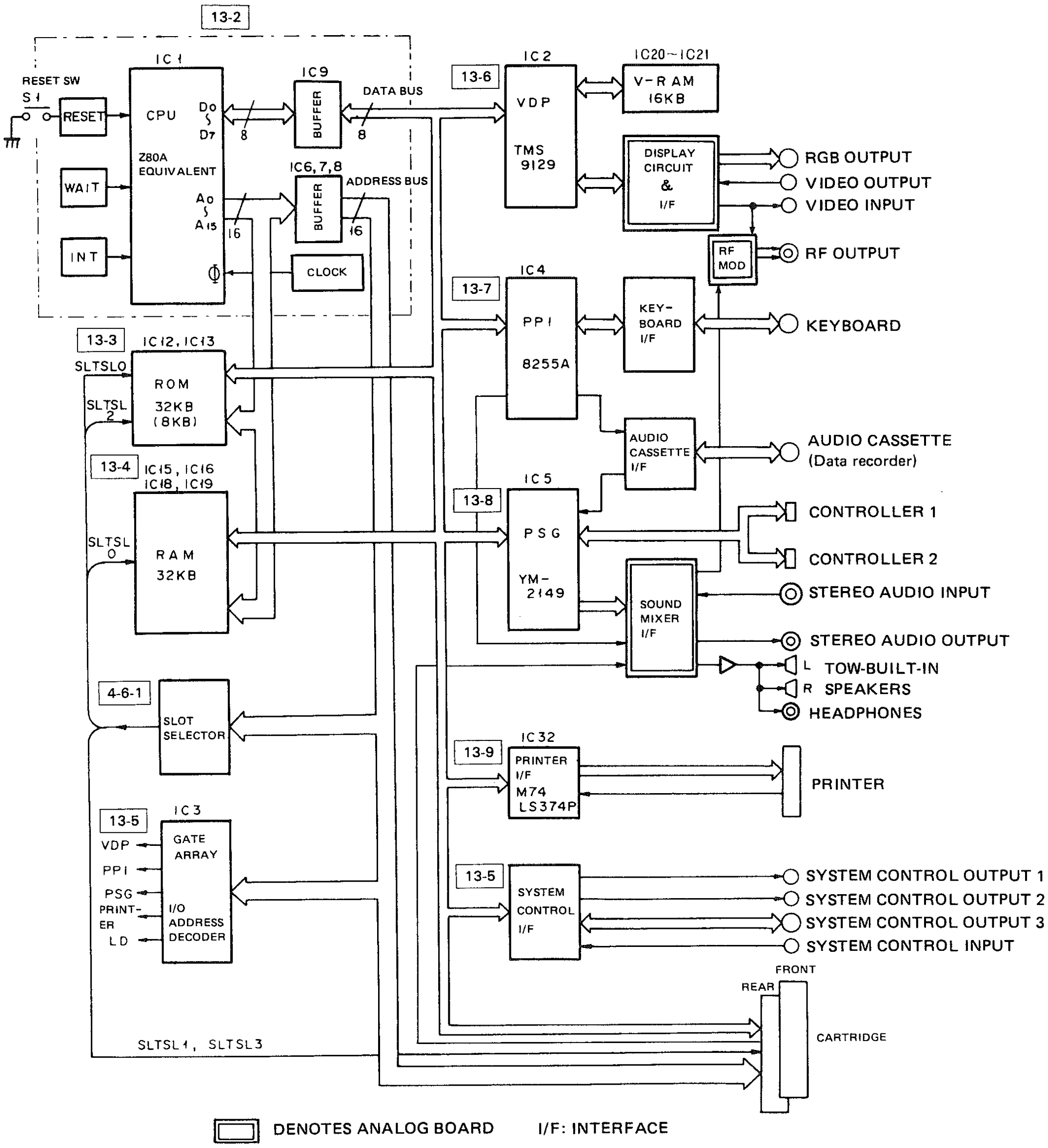


Fig. 13-1 Block diagram

13. 2. 1 CPU (Central Processing Unit)

The CPU (IC1) is an equivalent Z80A device (LH0080A).

13. 2. 2 System Clock

The system clock (3.58MHz) is generated by an oscillator consisting of a ceramic resonator X1, IC37(1/6), and IC8(1/6), and is supplied to the CPU, PSG, gate array, and cartridge slots.

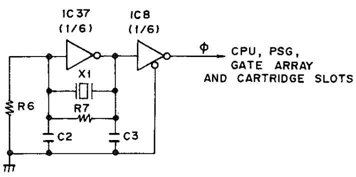
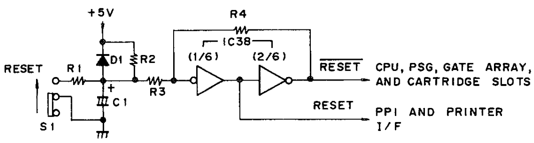


Fig. 13-2 System clock oscillator

13. 2. 3 Reset Circuit

The PX-7 is initialized by this circuit when the power is switched on or when the RESET switch (S1) is switched on. The CPU is reset by applying a active-low pulse. When the power is switched on, a pulse delayed by the period of time taken to charge up C1 by the leading edge of the power supply voltage is applied to the CPU. The CPU, PSG, gate array, and cartridge slots are reset by active-low, and the PPI and printer I/F are reset by active-high.



RESET PULSE GENERATED BY C1 CHARGING / DISCHARGING.
R1 : CURRENT LIMITING
D1 : C1 DISCHARGED WHEN POWER IS SWITCHED OFF.
R2 : C1 CHARGING (INCLUDING IC38 GATE LEAK CURRENT)
R1 AND R4 : POSITIVE FEEDBACK RESISTANCE (SCHMITT TRIGGER FORMED FOR STABLE ON/OFF SWITCHING)

Fig. 13-3 Reset circuit

13. 2. 4 WAIT Circuit

The WAIT circuit inserts a TW state (1 WAIT) between the T2 and T3 states in an M1 cycle (instruction fetch cycle) to ensure ROM or RAM accessing time on the basis of MSX standards. It is also possible to obtain a WAIT by WAIT request ($\overline{\text{EXT WAIT}}$) from an external source, applying the input via the slot section if necessary from the external device.

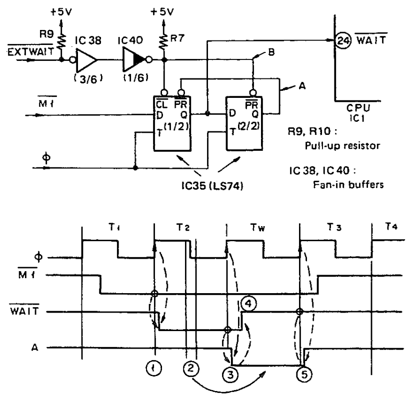


Fig. 13-4 Wait circuit

(1) IC35 (1/2) latches $\overline{M1}$ L at the leading edge of the T2 state ϕ in the M1 cycle. The IC35(1/2) Q output is thus switched to L.
(2) The CPU reads the L level applied to the $\overline{WAIT}$ pin from the IC35(1/2) Q output at the trailing edge of the T2 state ϕ, and subsequently generates the TW state.
(3) At the leading edge of the TW state ϕ, IC35 (2/2) latches the IC35(1/2) Q output L level by the D input, resulting in an L level output from IC35(2/2) Q.
(4) IC35(1/2) is preset by IC35(2/2) Q output L level, and the IC35(1/2) Q output (to $\overline{WAIT}$) is switched to H level.
(5) At the leading edge of the T3 state ϕ, IC35 (2/2) latches the IC35(1/2) Q output H level, resulting in an H level output from IC35(2/2) Q. The TW state is thus inserted.
(6) When the slot section $\overline{\text{EXT WAIT}}$ then becomes L, the IC40 output is switched to L, resulting in the IC35(1/2) $\overline{CL}$ and IC35(2/2) $\overline{PR}$ inputs also becoming L and the IC35(2/2) Q output becoming H. Therefore, an L level output is obtained from IC35(1/2) Q, and an L level input is applied to the $\overline{WAIT}$ pin of the CPU. The L output applied to this $\overline{WAIT}$ pin is maintained until the $\overline{\text{EXT WAIT}}$ status (switch to H) is cancelled (irrespective of ϕ and $\overline{M1}$).

13. 2. 5 Interrupt Circuit

This circuit generates three interrupts ($\overline{\text{EXTINT}}$, $\overline{\text{INTVDP}}$, and $\overline{\text{INTEXV}}$) to be applied to the CPU.

(1) $\overline{\text{EXTINT}}$ is an interrupt request signal applied from an external source via a slot.

(2) By using the VDP interrupt function once every 1/50th second by the interrupt routine supported by MSX BASIC, $\overline{\text{INTVDP}}$ processes key inputs by key scanning of the keyboard. The CPU internal timer is also activated by this input every 1/50th second to provide clock signals. This routine is also employed in processing inputs from the SUPERIMPOSE, VIDEO, and COMPUTER keys (unique Pioneer features).

(3) $\overline{\text{INTEXV}}$ generates an interrupt when the external video signal is stopped during superimpose or external video mode, thereby enabling switching from external to internal synchronization without picture disturbance.

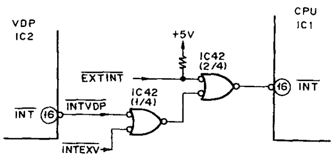


Fig. 13-5 Interrupt circuit

13. 2. 6 Address Bus

Due to fan-out reasons, the address bus is connected directly to the ROM/RAM circuits, but via buffers 74LS367 (IC6 thru IC8) to other circuits.

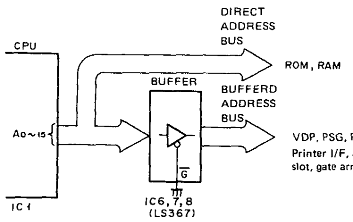
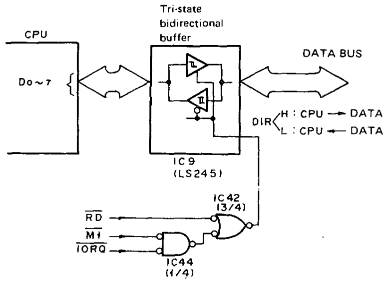


Fig. 13-6 Address bus

13. 2. 7 Data Bus

The data bus is connected to the various LSIs, ICs, and cartridge connectors via a bidirectional buffer 74LS245 (IC9).

Bidirectional buffers control the data direction depending on whether data is applied to or received from the CPU, this control being executed via the DIR pin in IC9. Data can be passed from the CPU to the data bus when an H level signal is applied to the DIR pin, and can be passed in the reverse direction when an L level signal is applied. The control signal applied to the DIR pin is formed by $\overline{\text{RD}}$, $\overline{\text{M1}}$, and $\overline{\text{IORQ}}$. L is applied to DIR (bus to CPU) when $\overline{\text{RD}}$, or both $\overline{\text{M1}}$ and $\overline{\text{IORQ}}$ are at L level, and H is applied (CPU to bus) in all other cases.



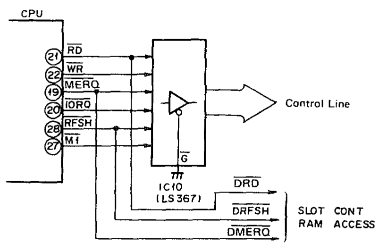
Data-bus-to-CPU when L applied to DIR due to $\overline{\text{RD}}$, or both $\overline{\text{M1}}$ and $\overline{\text{IORQ}}$, being at L level. CPU-to-data-bus in all other case.

* During interrupt request/acknowledge cycles, the direction is set to data-bus-to-CPU for the acknowledge cycle in order to read response vectors sent to the CPU from peripheral circuits.

Fig. 13-7 Data bus

13. 2. 8 Control Line

$\overline{\text{RD}}$, $\overline{\text{WR}}$, and other control signals from the CPU are connected to the various circuits via buffer LS367. $\overline{\text{DRFSH}}$, $\overline{\text{DMERQ}}$, and $\overline{\text{DRD}}$ are passed directly to the slot and RAM selector circuits bypassing the buffer to speed up slot selection and RAM accessing.



Slot signals and RAM access signals bypass buffer to speed up slot selection and RAM accessing.

Fig. 13-8 Control line

13. 3 ROM (Read Only Memory)

The ROMs used here include a 32K X 8-bit masking ROM YM-2301-23908 (IC12) with built-in MSX-BASIC (UK version) and a 8K X 8-bit masking ROM PD5031 (or EP-ROM M5L2764K-213) (IC13) with built-in P-BASIC (for extension BASIC).

13. 3. 1 ROM Accessing

The MSX-ROM is allocated to addresses 0000(H) thru 7FFF(H) of slot 0 (32K bytes), and is normally selected when the power is switched on. This MSX-ROM is selected when $\overline{MERQ}$=L, $\overline{RD}$=L, and $\overline{SLTSL0}$=L at memory addresses 0000(H) thru 7FFF(H) (A15→L). And as will be described later (13.7.1), an L output from $\overline{SLTSL0}$ is generated automatically when the power is switched on or when the RESET button is pressed, resulting in the MSX-ROM being selected and MSX BASIC being activated.

13. 3. 2 P-BASIC ROM Selection

The P-BASIC ROM is allocated to addresses 4000(H) thru 5FFF(H) of slot 2 (8K bytes), and is selected when a P-BASIC extension command is used or an interrupt is generated. The selection operation involves $\overline{CS}$ being switched to L when the 4000(H) thru 5FFF(H) memory is read at $\overline{SLTSL2}$→L.

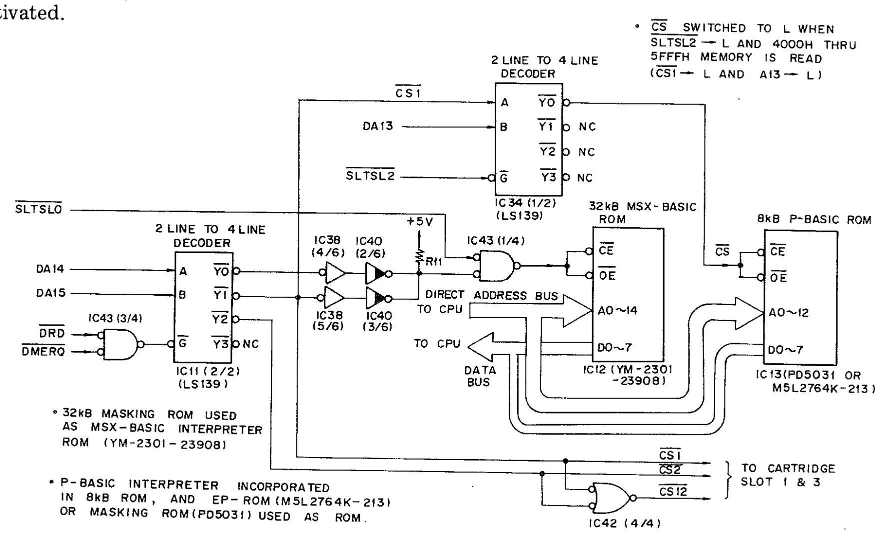


Fig. 13-9 ROM circuit

Table 13-1

$\overline{MREQ}$	$\overline{RD}$	$\overline{G}$	A15	A14	$\overline{Y_0}$	$\overline{Y_1}$ ($\overline{CS1}$)	$\overline{Y_2}$ ($\overline{CS2}$)	$\overline{CS12}$	$\overline{SLTSL0}$	$\overline{CE}$, $\overline{OE}$	
1	X	1	X	X	1	1	1	1	X	1	
X	1	1	X	X	1	1	1	1	X	1	
X	X	X	X	X	X	X	X	X	1	1	
0	0	0	0	0	0	1	1	1	0	0	MSX ROM Selection
0	0	0	0	1	1	0	1	0	0	0	
0	0	0	1	0	1	1	0	0	0	1	
0	0	0	1	1	1	1	1	1	0	1	

- ROM is selected when $\overline{MERQ}$, $\overline{RD}$, and $\overline{SLTSL0}$ are at L at memory addresses 0 thru 7FFFH (A15→L)
- The $\overline{CS1}$, $\overline{CS2}$, and CS12 output signals are passed to the connector section for slots 1 and 3.
- $\overline{CS1}$ (4000H thru 7FFFH) is also used as P-BASIC ROM selector signal.
- "0" in this table denotes L level, and "1" denotes H.

13. 4 RAM (RANDOM ACCESS MEMORY)

The main RAM consists of four 16K × 4-bit D-RAMs (dynamic RAMs) MB81416-12 (IC15, IC16, IC18, and IC19) for form a 32K byte area. An address multiplexer (IC14 and IC17) is used for RAM addressing purposes.

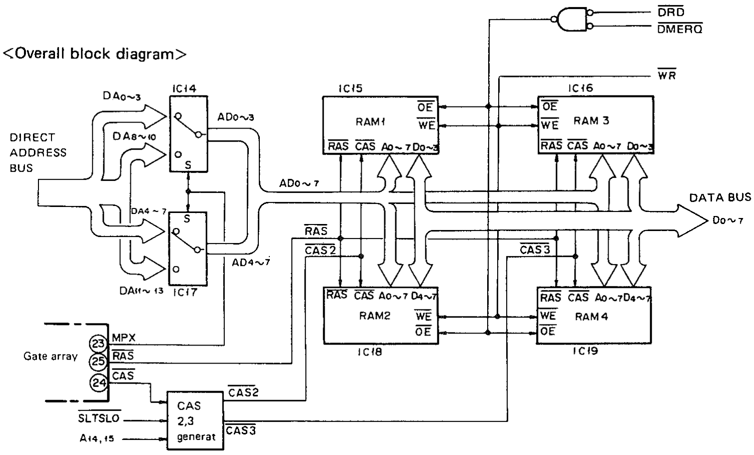


Fig. 13-10 Main RAM circuit

13. 4. 1 RAM Selection

(1) The main RAM is allocated to 8000H thru FFFFH of slot 0 (32K bytes) with D-RAMs (dynamic RAMs) used as the RAM elements. Refreshing is required when D-RAMs are used, and because of restrictions on the number of package pins, addressing is divided into two steps. This in turn requires the use of $\overline{RAS}$ (row-address strobe) and $\overline{CAS}$ (column-address strobe) control signals plus various MPX signals for the multiplexer. These signals are generated in the gate array.

(2) The MPX signal is used in row/column address switching prior to passing addresses to the RAM.

(3) Although the $\overline{RAS}$ signal is passed via a logic circuit for reasons related to the gate array, it may be considered as equivalent to the $\overline{MERQ}$ signal.

(4) Apart from the refresh cycle, the $\overline{MPX}$ signal is switched to H level at the leading edge of the first ϕ (clock) after $\overline{MERQ}$ is switched to L level, and is switched to L level when $\overline{RFSH}$ is L or at the leading edge of the first ϕ after $\overline{MERQ}$ is switched to H.

(5) $\overline{CAS}$ is switched to L at the trailing edge of the first ϕ after MPX is been switched to H, and is switched to H when $\overline{MERQ}$ is switched to H.

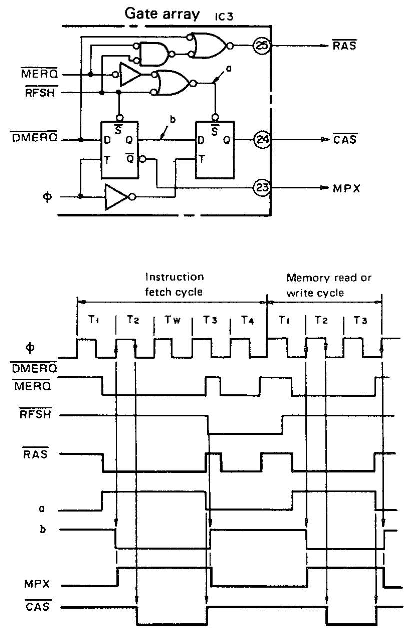


Fig. 13-11 RAM selection

13. 4. 2 CAS Decoder

Since four 16K × 4-bit D-RAMs are used as the main RAM (consisting of two 16K byte RAM pairs with two D-RAMs per pair to make 32K bytes), the $\overline{CAS}$ signal from the gate array (IC3) is decoded by $\overline{SLTSL0}$, A14, and A15, and is subsequently divided into $\overline{CAS2}$ and $\overline{CAS3}$ generated at 8000H thru BFFFH and C000H thru FFFFH of slot 0. These two signals are then applied to the respective D-RAM pairs.

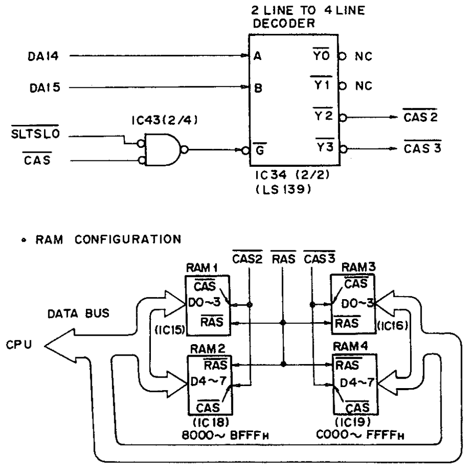


Fig. 13-12 CAS decoder

13. 4. 3 Address Multiplexer

A 14-bits address lines (A0 thru A13) are required to specify 16K bytes (2^{14}) addresses. D-RAMs, however, are only equipped with address input pins for up to 8 bits (A0 thru A7). Hence, A0 thru A13 is divided into row address (A0 thru A7) and column address-(A8 thru A13) with addressing operations being executed in two steps.

(1) Addresses are divided into row and column addresses by multiplexer controlled by the MPX signal.

(2) In the D0RAM, the row or column addresses are identified by the $\overline{RAS}$ or $\overline{CAS}$ signal.

(3) Column addresses A8 thru A13 are two bits shorter than row addresses. The address distribution method is outlined in Table 13-2 below.

<Address multiplexer>

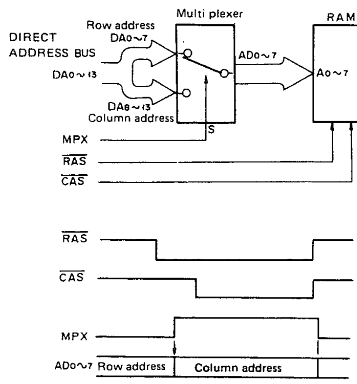


Fig. 13-13 Address multiplexer

Table 13-2 Address distribution

AD	7	6	5	4	3	2	1	0
Row	A7	A6	A5	A4	A3	A2	A1	A0
Column	—	A13	A12	A11	A10	A9	A8	—

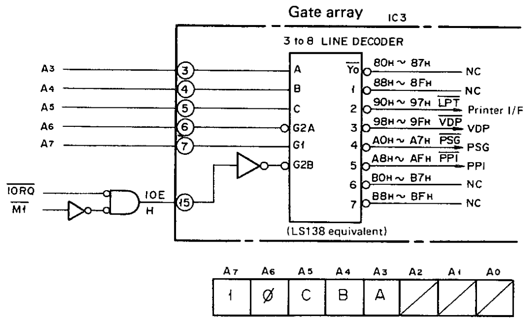
13. 5 I/O CONTROL

13. 5. 1 I/O Address Decoder

If the CPU is to access a memory or I/O, either $\overline{MERQ}$ or $\overline{IORQ}$ must become active (L). If an I/O is accessed by program, $\overline{IORQ}$ becomes L, and the output from the CPU is $\overline{WR}$=L if the command is written in the I/O, or $\overline{RD}$=L if the I/O status is read. When $\overline{IORQ}$ is L apart from during an M1 cycle (that is, when an I/O request is generated outside an interrupt acknowledge cycle), the I/O address decoder circuit is enabled by IOE being changed to H. I/O access signals are thus generated at 8-byte intervals by decoding addresses A3 thru A7.

When A7 is H and A6 is L in an actual circuit, A3 thru A5 is decoded by a 3-to-8-LINE decoder, and I/O access signals generated at 8-byte intervals from 80H to BFH are allocated to each I/O. As a result, I/O addresses 90H thru 97H are allocated to the printer I/F, 98H thru 9FH to the VDP, A0H thru A7H to the PSG, and A8H thru AFH to the PPI.

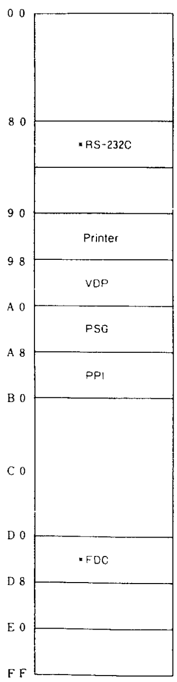
The I/O map is outlined in the table below.



- I/O access signals are generated at 8-byte intervals from 80(H), use being made of the signals from 90(H) to AF(H).
- Since A0 thru A2 are not decoded here, an 8-byte image is obtained. Therefore, decoding in more detail may be necessary in some cases when accessing different divices.

Fig. 13-14 I/O Address decode circuit

Table 13-3 I/O address allocation



	RW	Details	Remarks
&H98	W	Data write into VRAM	TMS9129NL or equivalent
	R	Data read from VRAM	
&H99	W	Command, address set	
	R	Status read	
&HA0	W	Address latch	AY-3-8910 or equivalent
&HA1	W	Data write	
&HA2	R	Data read	
&HA8	W	Port A data write	8255A or equivalent
	R	Port A data read	
&HA9	W	Port B data write	
	R	Port B data read	
&HAA	W	Port C data write	
	R	Port C data read	
&HAB	W	Mode set	
&H90	W	Strobe output (b0)	latch output
	R	Status input (b1)	"1" is BUSY
&H91	W	Print data	latch output

I/O addresses from 80 to FF area prescribed as above for system use. Empty columns are system reserves.

*I/O addresses marked with an asterisk are for optional equipment.

13.5.2 Extension I/O Interface

The I/O address allocation is stipulated by MSX (see Table 13-3), and no other I/O can be allocated to an I/O address. If a hypothetical I/O register is set in the memory address of a suitable slot by the memory mapped I/O method, other I/Os can be set in this register. The extension I/O is placed in memory address 7FFEH (LCON register) and 7FFFH (VCON register) of slot 2 by the memory mapped I/O method for exchange with the CPU.

The extended I/O interface is used in video, audio, and system control with accessing executed by A0 thru A15, $\overline{\text{SLTSL2}}$, $\overline{\text{WR}}$, and $\overline{\text{RD}}$ to generate the following signals.

$\overline{\text{LCONW}}$ L when 7FFEH writing
$\overline{\text{LCONR}}$ L when 7FFEH reading
$\overline{\text{VCONW}}$ L when 7FFFH writing
$\overline{\text{VCONR}}$ L when 7FFFH reading

The bit allocation for memory addresses 7FFEH and 7FFFH is outlined in Tables 13-4 and 13-5.

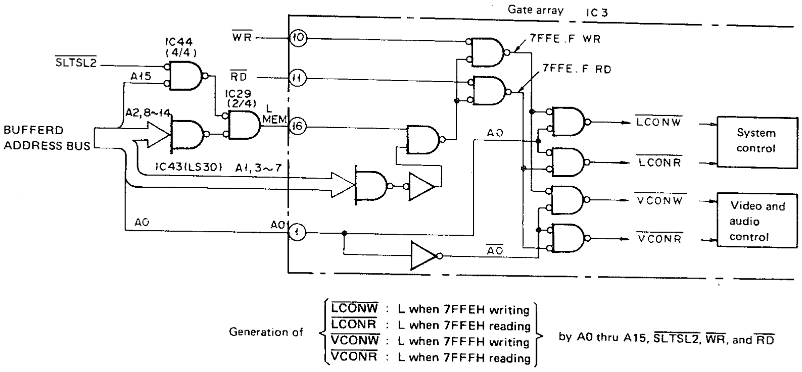


Fig. 13-15 Extended I/O interface

Table 13-4 Expansion I/O resisters (Slot #2)
LCON register <7FFE (16)>

Bit	RW	Signal	Function
7	R	$\overline{\text{ACK}}$	Significant with acknowledge 1→0 with respect to remote control signal transmission
6			Not used
1			Not used
0	R	RMCLOK	Clock produced by dividing CLK1/CLK2 frequency by 128
	W	$\overline{\text{REM}}$	High output with bit serial data output generated in synchronization with RMCLK

Table 13-5 Expansion I/O registers (slot #2)
VCON resister <7FFF (16)>

Bit	RW	Signal	Function
7	R	EXTV	Status indicating availability of external video signal. Low when available; high when not available.
	W	Mute	Line input signal muting
6			Not used
1			Not used
0	R	INTEXV	Interrupt available with interrupt flag 1 when external video signal is OFF. Set to 0 when read.
	W	OVERPLAY	Hardware selection signal of superimpose/non-superimpose mode; 0 for superimpose, 1 for non-superimpose

(1) Video control circuit

- $\overline{\text{EXTV}}$ reading

① $\overline{\text{EXTV}}$ is a status signal indicating the presence/absence of an external video signal (L level when present)
② $\overline{\text{EXTV}}$ is read by the CPU when bit 7 of the VCON register is read.
③ Example:
The VCON register contents are placed in register A by

LD A, (7FFFH)

and the $\overline{\text{EXTV}}$ status is indicated by D7.

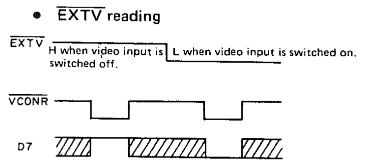


Fig. 13-16 $\overline{\text{EXTV}}$ reading timing

- $\overline{\text{VOVLY}}$ generation

① The $\overline{\text{VOVLY}}$ control signal used in computer mode and superimpose/external video mode switching is only switched to L when an external video signal is applied ($\overline{\text{EXTV}}$ at L) with L written in bit 0 of the VCON register.
② When $\overline{\text{RESET}}$ is switched to L, $\overline{\text{VOVLY}}$ is switched to H with point E in Fig. 13-19 at H.
③ The D0 status (L or H) is latched by the leading edge of $\overline{\text{VCONW}}$, and the Q output (E) is ORed with $\overline{\text{EXTV}}$ to obtain the $\overline{\text{VOVLY}}$ signal.

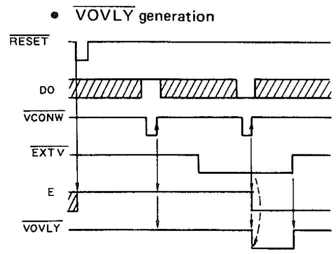


Fig. 13-17 $\overline{\text{VOVLY}}$ generation timing

- $\overline{\text{INTEXV}}$ generation

① The $\overline{\text{INTEXV}}$ and INTEXV signals are generated when the external video signal stops in superimpose or external video mode. $\overline{\text{INTEXV}}$ serves as the CPU interrup signal, and INTEXV serves as the corresponding status signal.
② Since point A is at H and point B at L when $\overline{\text{RESET}}$ is applied, point C and point D are switched to H, resulting in $\overline{\text{INTEXV}}$ also being switched to H. And when the VCON register is read, INTEXV=0 is obtained from bit 0.
③ When $\overline{\text{EXTV}}$ is changed from L to H (that is, when the external video signal is stopped), point C is kept at L from the leading edge of the next ϕ up to the trailing edge of the next ϕ after that, thereby resulting in point D becoming L and point $\overline{\text{D}}$ H.
④ If point E is L (designation of superimpose or external video mode), $\overline{\text{INTEXV}}$ is switched to L to generate a CPU interrupt.
⑤ INTEXV=1 is obtained from bit 0 when the VCON register is read during the interrupt processing routine, thereby indicating that the interrupt is from $\overline{\text{INTEXV}}$. After completing the read operation, point D is changed to H and point $\overline{\text{D}}$ to L by the VCONR leading edge, resulting in $\overline{\text{INTEXV}}$ being reverted to H to cancel the interrupt.

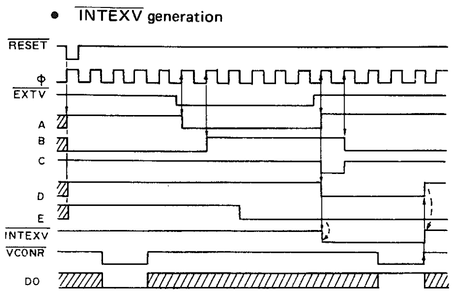


Fig. 13-18 INTEXV generation timing

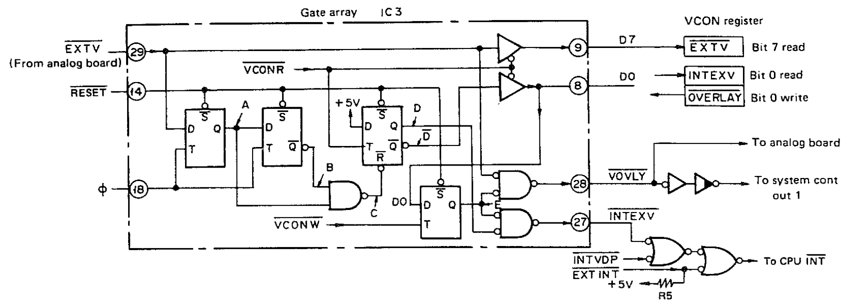


Fig. 13-19 Video control circuit

(2) Audio control circuit
Muting of external stereo audio inputs is switched on and off by this circuit. Left and right channel muting signals (LMUTE and RMUTE) are generated by output of VCON register bit 7 write and PPI PC port bit 4 (PC4). To latch PC4 by using the LMUTE leading edge during right channel muting control, LMUTE has to be changed from L to H. An integrating circuit (R319/C305) is used to prevent response in the left channel muting circuit (Q303/Q305) during this L → H change. And to ensure equal response times in both left and right channels, an integrating circuit (R320/C306) is also included in the right channel muting circuit (Q304/Q306).

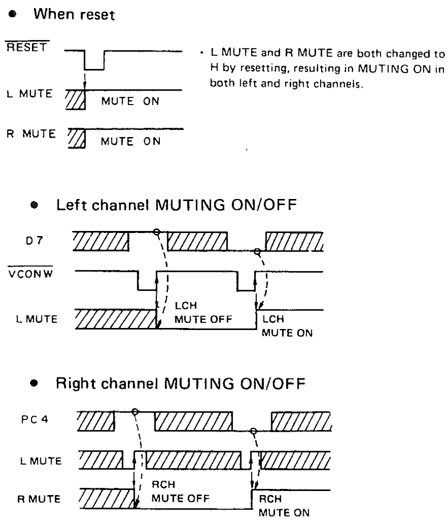


Fig. 13-20

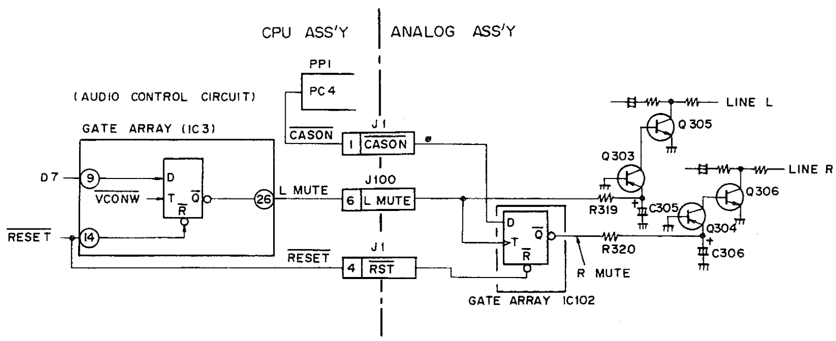


Fig. 13-21 Audio control circuit and timing

(3) System control circuit

(3-1) Reference clock generator

The reference clock generator generates timing pulses used in software generation of control pulses for PIONEER'S standard remote control (SEED, LD-700) and LD-1100 series remote control units.

Although two reference clocks are required (455kHz for LD-1100, and 500kHz for PIONEER'S standard remote control) for the different pulse widths in standard and LD-1100 remote control units, the LD-1100 is capable of functioning adequately at 500kHz. Therefore, the reference clock has been set to 500kHz in a circuit consisting of ceramic resonator (X 2) and IC 37 (3/6, 4/6). The frequency of the 500kHz reference clock 128 (see Waveform e in Fig. 13-22) and is subsequently read by the CPU via bit 0 of the LCON register.

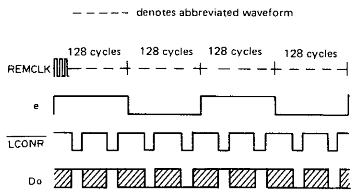


Fig. 13-22 Reference clock generation and timing

(3-2) Remote control pulse generator

(1) The remote control code is written (by software) in bit 0 of the LCON register on the basis of the timing pulse generated by the reference clock generator.

(2) This latched output is UREMO which serves as the source signal for wired remote control.

(3) CREMO is generated by on/off switching of the output obtained by dividing REMCLK by 12 based on UREMO.

(4) CREMO is an infra-red LED drive signal connected by coupler cord for infra-red remote control operation. (Q9 is a driver transistor which is no longer necessary with LD-1100 since direct connection to the control terminal is possible.)

(5) $\overline{\mathrm{EXTREMO}}$ is a universal wired remote control output.

(6) $\overline{\mathrm{LREMO}}$ is a wired remote control signal output for an LD-700 unit, and $\overline{\mathrm{EXTREMI}}$ is a wired remote control input for remote control signals passed to an LD-700 unit from an SD-26 unit.

(7) Either $\overline{\mathrm{UREMO}}$ or $\overline{\mathrm{EXTREMI}}$ is selected by $\overline{\mathrm{LREMO}}$ depending on the SELCONT status.

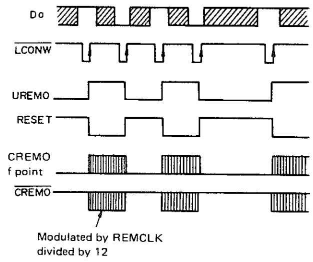


Fig. 13-23 Remote control pulse generation and timing

Selection Operation

(1) When SELCONT is +5V

- UREMO is changed to L, Q4 is turned on, Q5 is turned off, and $\overline{\mathrm{LREMO}}$ is changed to H via D16 irrespective of the $\overline{\mathrm{EXTREMI}}$ L/H status.
- UREMO is changed to H, Q4 is turned off, Q5 is turned on, and $\overline{\mathrm{LREMO}}$ is changed to L via R53 irrespective of the $\overline{\mathrm{EXTREMI}}$ L/H status.

(2) When SELCONT is 0V

- UREMO is changed to L when no remote control signal is sent, resulting in Q4 being turned off, Q5 turned off, and output of $\overline{\mathrm{EXTREMI}}$ to $\overline{\mathrm{LREMI}}$.

SELCONT is a power supply voltage linked to the through switch.

(3-3) Other circuits

(1) The L/H status of the acknowledge signal (LACK) (changed according to remote control signals from LD-700) is read by the CPU via bit 7 of the LCON register. (See Fig. 13-24.)

(2) SELECTO is a control output passed to LD-700 units.
Wired remote control is valid when SELECTO is L, and infra-red remote control is valid when SELECTO is H.

(3) That is, SELECTO is changed to L to enable LREMO. (See Fig. 13-25.)

(4) If there is no SELECTI input, SELECTO is changed to L to enable LREMO when SELCONT is +5V, but is changed to H to disable LREMO when SELCONT is 0V.

(5) The SELECTI input is applied to the stereo mini-jack R terminal (the L terminal being for EXTREMI inputs).

(6) If the SD-26 control output is connected by mini-plug to the stereo mini-jack as shown in Fig.13-25, SELECTI makes contact with the plug GND and is consequently changed to L.

(7) Therefore, when SELCONT is changed to L, SELECTO can be changed to L and EXTREMO can be enabled.

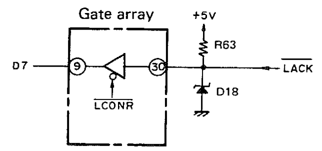


Fig. 13-24 Acknowledge read circuit

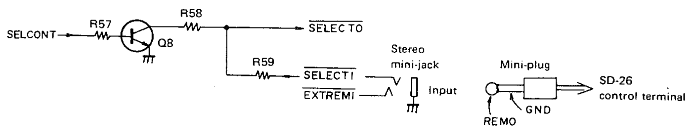


Fig. 13-25 Select circuit

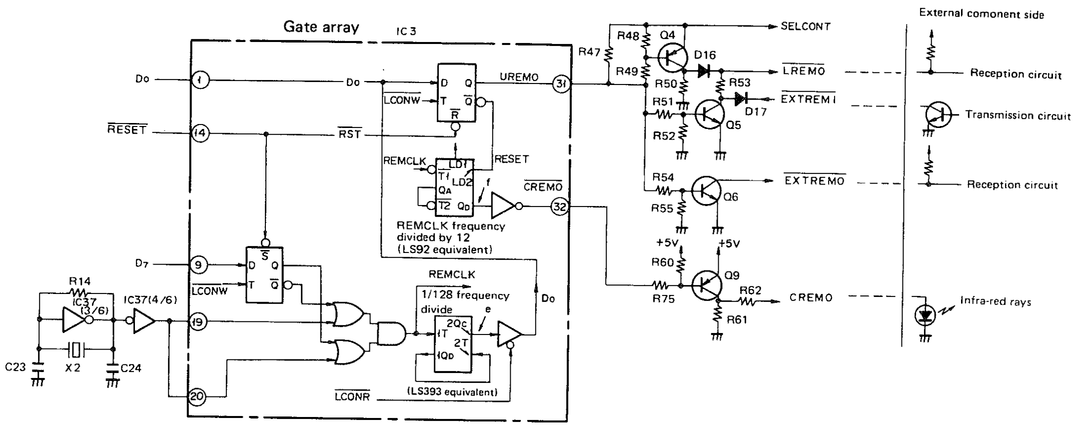


Fig. 13-26 System control circuit

13. 6 VDP (VIDEO DISPLAY PROCESSOR)

The VDP (TMS9129NL) is accessed at VDP=L with data transfer being controlled by CSW, CSR, and MODE.

CSW: Write signal changed to L when data is written from CPU to VDP

CSR: Read signal changed to L when data is read from CPU to VDP

MODE: L level when reading/writing V-RAM to/from CPU, and H in other cases.

CPU address A0 is normally connected to MODE, and the VDP and V-RAM are accessed separately depending on the A0 value when the VDP is accessed.

Table 13-6

MODE (AO)	CSR	CSW	Status
L	H	L	Direct writing from CPU to V-RAM (data set at CSW leading edge)
L	L	H	Direct reading of V-RAM data to CPU
H	H	L	Writing from CPU to VDP
H	L	H	Reading of VDP status to CPU

The RESET/SYNC input is (1) 0V when RESET is L, (2) 5V when RESET is H and SYNC is L (+12V divided by R12 and R13), (3) and 12V when RESET and SYNC are both H.

Table 13-7

RESET	SYNC	RESET/SYNC	Operation
L	X	0V	When reset (when power is switched on or when RESET switch is pressed)
H	L	5V	During normal operation
H	H	12V	When external synchronizing signal SYNC is applied during superimpose or external video mode

(1) With RESET/SYNC leading edges serving as horizontal synchronizing pulses, the VDP internal counter is reset in a horizontal synchronous state.

(2) And with synchronizing pulses greater than 7.2 μsec serving as vertical synchronizing pulses, the internal vertical counter is set in a vertical synchronous state.

(3) The INT output (VDP interrupt signal) generates L level pulses at the end of each display screen scanning operation (that is, at every 1/50th sec synchronized with VSYNC). And as INTVDP, the INT output is also connected to the CPU interrupt pin to be used as a 1/50th sec timer interrupt.

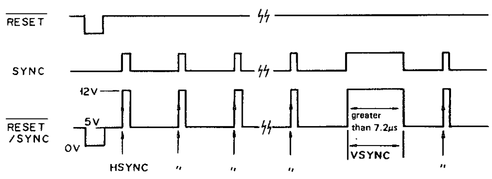


Fig. 13-27 RESET/SYNC input waveform

The VDP clock (10.68MHz) rectifies the CLK signal at R74, D23, and C55, this then being applied to X'TAL 1 of VDP via an inverter at a duty of almost 50%.

A 16K byte V-RAM memory is formed by two 16K X 4-bit DRAMs (TMS4416-15NL equivalent). This V-RAM is accessed by RAS, CAS, and WE in the same way as the main RAM.

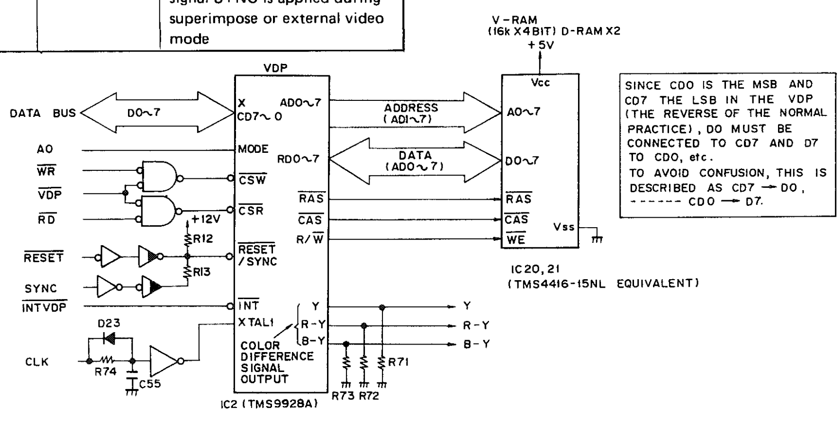


Fig. 13-28 VDP circuit

13. 7 PPI (PROGRAMMABLE PERIPHERAL INTERFACE)

PPI is a parallel interface IC equipped with three 8-bit input/output ports (PA, PB, and PC). The role of each port is summarized below.

PA port: Generation of slot selector signal
PB port: Reading of key inputs from the keyboard
PC port: Four lower bits PC0 thru PC3:
Key scanning signal generation
Four higher bits
PC6: CAPS lamp switching
PC4: Cassette I/F remote relay control
PC5: Cassette data writing
PC7: Key click tone source

Each PPI port is selected on the basis of the status of A0, A1, $\overline{WR}$, and $\overline{RD}$ when $\overline{PPI}$=L and $\overline{CS}$=L (see Table 13-8). The formation of address images is prevented by using A2 in $\overline{CS}$. Note that the MSX is used in mode 0.

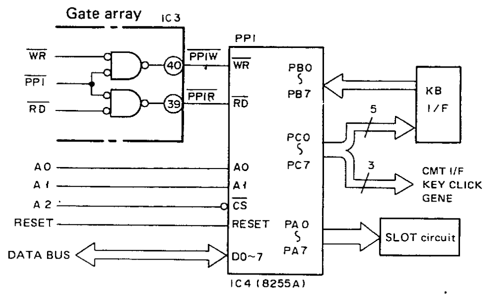


Fig. 13-29 PPI circuit

Table 13-8

I/O address	A2(CS)	A1	A0	PPIW	PPIR	Operation		
A8	0	0	0	0	1	BD BUS ←— PA	R	
	0	0	0	1	0	BD BUS —→ PA	W	Slot selection
A9	0	0	1	0	1	BD BUS ←— PB	R	Key input read
	0	0	1	1	0	BD BUS —→ PB	W	
AA	0	1	0	0	1	BD BUS ←— PC	R	
	0	1	0	1	0	BD BUS —→ PC	W	Key scanning output, cassette, key click
AB	0	1	1	0	1	Inhibited	R	
	0	1	1	1	0	Mode setting	W	
	X	X	X	1	1			
	1	X	X	X	X			

"0" in this table denotes L, and "1" denotes H level

Table 13-9 PPI bit allocation

Port	Bit	I/O	Signal	Description
A (PA)	0 1	Output	CS0L CS0H	0000H thru 3FFFH address slot designation signal
	2 3		CS1L CS1H	4000H thru 7FFFH address slot designation signal
	4 5		CS2L CS2H	8000H thru BFFFH address slot designation signal
	6 7		CS3L CS3H	C000H thru FFFFH address slot designation signal
B (PB)	0 ~ 7	Input		Keyboard return signal
C (PC)	0 1 2 3	Output	KB0 KB1 KB2 KB3	Keyboard scan signal
	4		$\overline{CASON}$	Cassette motor control (ON when L)
	5		CASW	Cassette write signal
	6		$\overline{CAPS}$	CAPS lamp signal (ON when L)
	7		SOUND	Sound output generated by software

13. 7. 1 Slot Selector Circuit

The slot selector circuit divides the 64K byte memory area into four parts of 16K bytes each according to the values of the PPI PA ports PA0 thru PA7, and allocates each part to a corresponding slot 0 thru 3.

When the system is reset, all PPI ports become input ports at high impedance, resulting in the $\overline{SLTE}$ signal becoming H for automatic selection of slot 0 (to activate MSX-BASIC as indicated in Table 13-10*). Once the PPI is accessed, however, $\overline{SLTE}$ becomes L to enable slots to be selected according to PA port data.

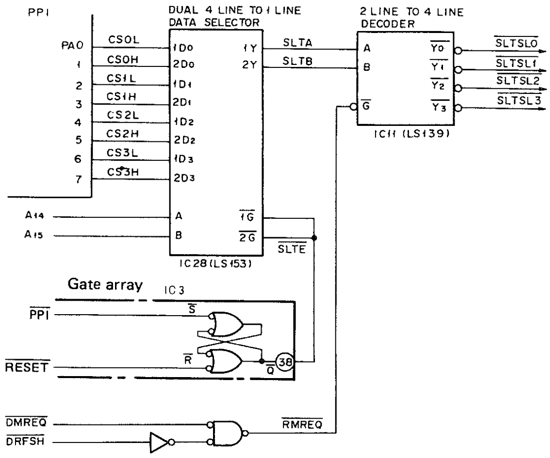


Fig. 13-30 Slot selector circuit

Table 13-10

Memory address	A15	A14	$\overline{SLTE}$	SLTB	SLTA	CSnH	CSnL	$\overline{RMREQ}$	$\overline{SLTSL}$ 0	1	2	3
0000 ~ 3FFF	0	0	0	CS0H	CS0L	0	0	0	0	1	1	1
						0	1	0	1	0	1	1
						1	0	0	1	1	0	1
						1	1	0	1	1	1	0
4000 ~ 7FFF	0	1	0	CS1H	CS1L	0	0	0	0	1	1	1
						0	1	0	1	0	1	1
						1	0	0	1	1	0	1
						1	1	0	1	1	1	0
8000 ~ BFFF	1	0	0	CS2H	CS2L	0	0	0	0	1	1	1
						0	1	0	1	0	1	1
						1	0	0	1	1	0	1
						1	1	0	1	1	1	0
C000 ~ FFFF	1	1	0	CS3H	CS3L	0	0	0	0	1	1	1
						0	1	0	1	0	1	1
						1	0	0	1	1	0	1
						1	1	0	1	1	1	0
x X	X	X	1	0	0	0	0	0	0	1	1	1
X	X	X	X	X	X	X	X	1	1	1	1	1

"0" in this table denotes L, and "1" denotes H level.

- Slot selection

Slots are selected by PA ports in the following way. The function of the CSnH and CSnL signals (where n = 0 to 3) for PA0 thru PA7 is to specify addresses for each 16K bytes, and to specify the corresponding slots (0 thru 3) for those addresses. These CSnH/L signals can be considered as CSn and SLT H/L elements in the following way.

(1) CSn (where n = 0 to 3) specified addresses for each 16K bytes (page φ thru 3)

(2) SLTH and SLTL specify slots 0 thru 3 in two-bit binary

That is, the CSnH/L signals determine which 16K bytes in the slot 0 thru 3 × 64K byte memory matrix is to be used to form a 64K byte × 1 memory which can be handled by the CPU.

For example, to form a 64K byte memory area using the four 16K byte memory areas indicated by the shaded sections (a, f, k, and p) in Fig. 13-31,

the required conditions are:—
CS0 and SLTH set to 0 and SLTL set to 0
CS1 and SLTH set to 0 and SLTL set to 1
CS2 and SLTH set to 1 and SLTL set to 0
CS3 and SLTH set to 1 and SLTL set to 1
That is,

PA0 = CS0L → 0	If 11100100 = E4(H) is set in PA0 thru
PA1 = CS0H → 0	PA7, the CPU can handle the memory
PA2 = CS1L → 1	area shown in the diagram below as a
PA3 = CS1H → 0	consecutive 64K byte memory.
PA4 = CS2L → 0	This method also prevents the danger
PA5 = CS2H → 1	of bus collisions if identical
PA6 = CS3L → 1	address memories in different slots
PA7 = CS3H → 1	are accessed simultaneously.

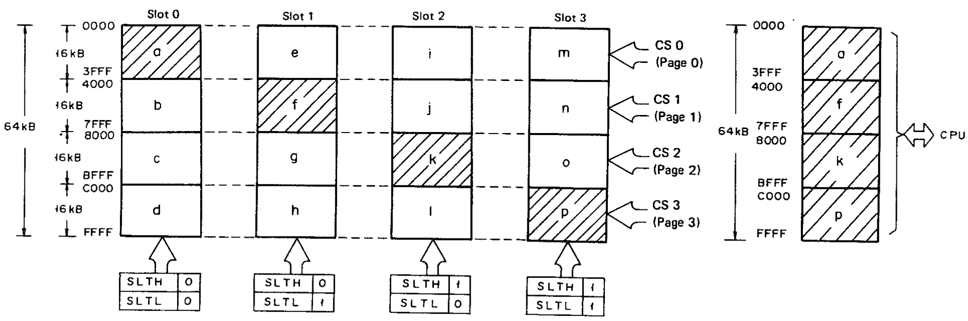


Fig. 13-31 Slot selection

13. 7. 2 Cassette Interface Section

● Input circuit

When the PPI pin 13 $\overline{\text{CASON}}$ output is changed to H level, Q2 is turned off and relay RY1 is put into break status. In this condition, REM+/– is open and the cassette recorder motor is stopped.

The IC33(2/2) output is connected to the IC33(1/2) comparator input via a clamp circuit (to prevent excessive inputs) consisting of R34, D4, D3, C33, and C34, thereby resulting in input of LD DATA to IC33(1/2). The IC33(2/2) CPE interface serves as an amplifier to ensure that the LD DATA is at the same level as the CMT IN signal. IC33(1/2) also forms a schumitt amplifier with positive feedback via R27 and R26.

When the PPI pin 13 $\overline{\text{CASON}}$ output is changed to L level, Q2 is turned on and the relay is put into make status. REM+/– is shorted and the motor is switched on, resulting in the input from CMT IN being applied to IC33(1/2).

● Output circuit

The PPI pin 12 CASW (PC5) output is passed via a bandpassfilter consisting of C30, C31, and R22 thru R24, resulting in an output quasi-audio signal being passed to CMT OUT.

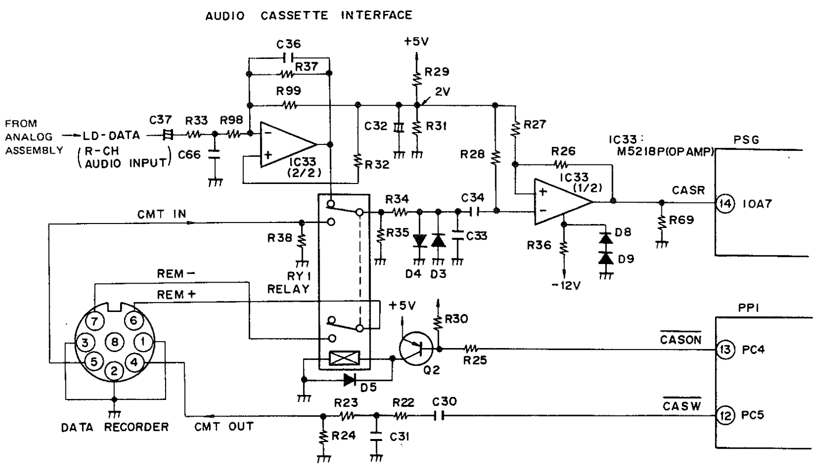


Fig. 13-32 Cassette interface circuit

13. 7. 3 Keyboard I/F

The number of leads in the connecting cable to the separated keyboard is reduced by using a partially bidirectional bus line.

The bidirectional section of the bus line includes KX0, KX1, KX2, KX4, and YA thru YD, thereby reducing the number of leads in a bus line requiring 17 leads to 13. Bus line control involves enabling IC45 by scan data output passed from the CPU to the PC port, and passing YA thru YD to the bus. Bus collisions are avoided by disabling U2 in advance. IC45 is disabled after YA thru YD is latched by U4. This is followed by enabling U2, passing the X0, X1, X2, and X4 key inputs to the bus, and reading from the PB port.

The reason for delay 1 is to enable IC45 until YA thru YD has been completely latched by U4. And the reason for delay 2 is to enable U2 after IC45 has been disabled.

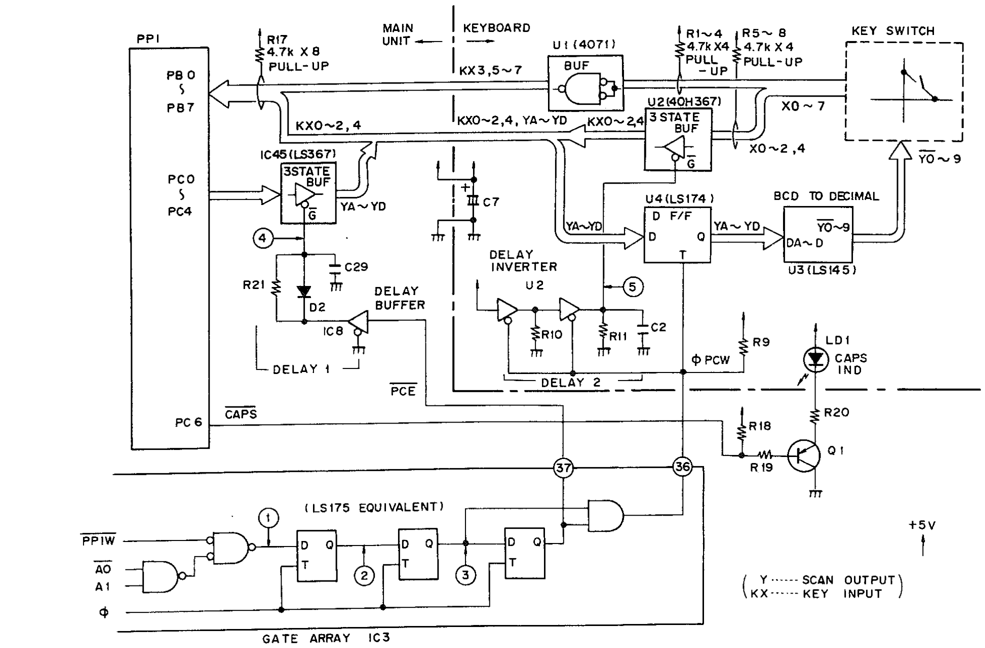


Fig 13-33 Keyboard interface circuit

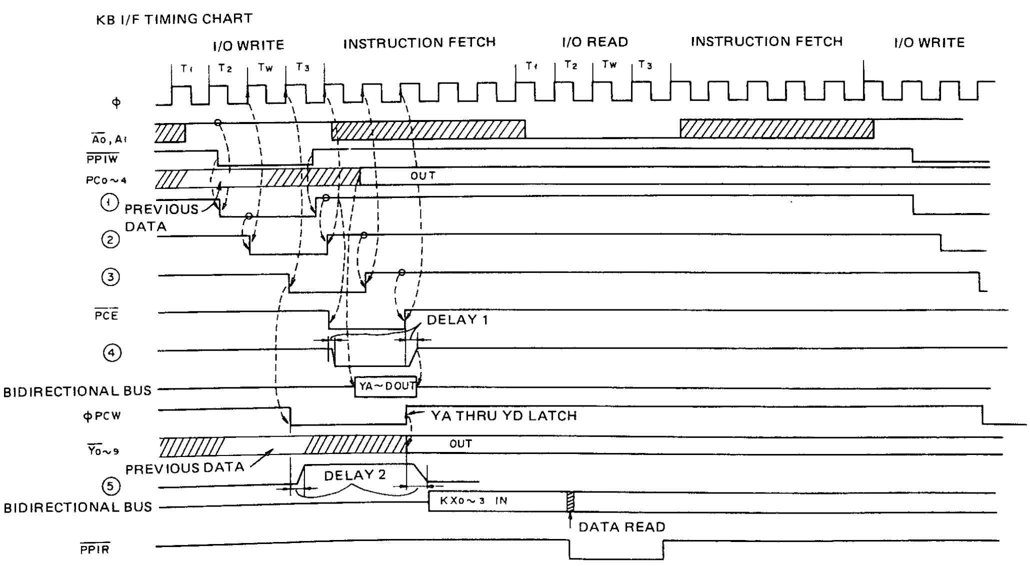


Fig. 13-34 Keyboard interface timing chart

13. 8 PSG (PROGRAMMABLE SOUND GENERATOR)

The PSG (IC5) circuit is the Yamaha YM-2149. This LSI is up compatible with the higher ranking AY-3-8910 from the GI Company, and features a clock frequency divider (1/2) to enable direct input of the system clock. The PSG has three independent sound outputs A, B, and C which are connected to left and right channels by a matrix circuit in the PX-7 for output to speakers via a mixing amplifier (IC110) and power amplifiers (IC111 and IC112). And in addition to a sound generator function, this LSI also features two 8-bit parallel I/O ports (IOA and IOB) used in a controller I/F for joystick and tablet connections.

The PSG is accessed by BDIR and BC1 with BC2 and A8 at H level and A9 at L level. (A2 is applied to the A9 input to prevent generation of address images.) BDIR and BC1 are both changed to H by writing the I/O address A0 (H), and the register address is then latched by the PSG. Data writing is executed when BDIR is changed to H with BC1 remaining at L by A1(H) writing, and data reading is executed when BC1 is changed to H with BDIR remaining at L by A2(H) reading. The timing for these operations is outlined in Fig. 13-36

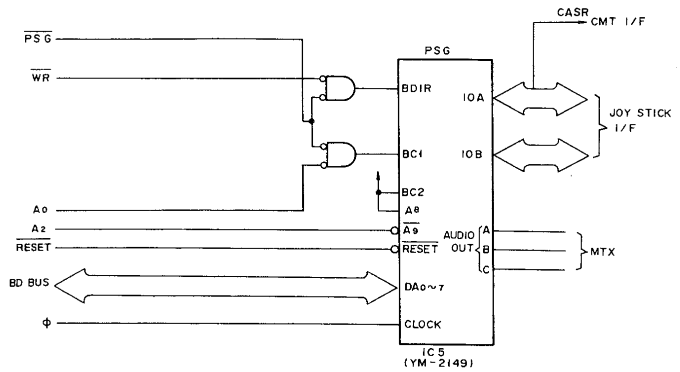


Fig. 13-35 PSG circuit

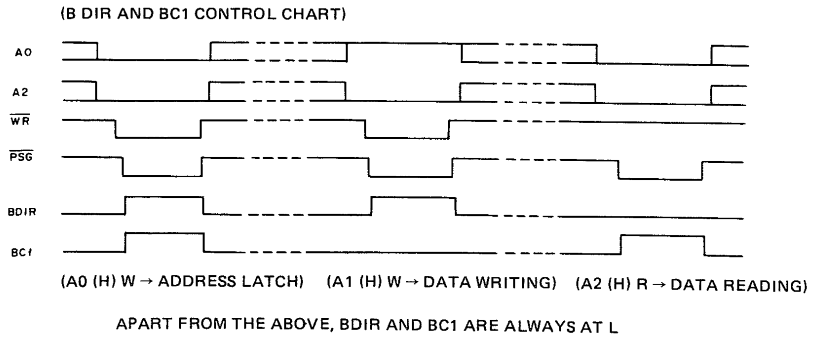


Fig. 13-36 PSG BDIR, BCI control chart

13. 8. 1 Joystick I/F

The controller 1 and controller 2 universal input/output port devices are equipped with four input bits, two input/ output bits, and one output bit in addition to 5V and GND for joystick and tablet connections. The controller 1 and 2 ports formed by using PSG IOA and IOB are used in the following ways.

(1) IOA are used as "input only". Pins 1 thru 4 of controllers 1 and 2 are connected to pins IOA0 thru IOA3 via the data selector IC 74LS157 (IC30). Likewise, pins 6 and 7 of controllers 1 and 2 are connected to pins IOA4 and IOA5 via the data selector IC 74LS157 (IC31). The IOA7 pin is also used as a CMT serial input port, while the IOA6 input is not used in this case, and is left at H level.

(2) IOB are used as "output only". The IOB0 thru IOB3 pins are connected by open collector via respective buffers 74LS04 (IC39) and 74LS05 (IC41), IOB0 and IOB1 being connected to pins 6 and 7 of controller 1 and IOB2 and IOB3 being connected to pins 6 and 7 of controller 2. IOB6 is used as a selector signal in controller 1 and 2 switching (L: controller 1, H: controller 2). IOB4 and IOB5 are connected to pin 8 of controllers 1 and 2 respectively, and the IOB7 output is not used.

(3) When a joystick is used, pins 1 thru 4 are used as forward/back and left/right key inputs, pins 6 and 7 are used as trigger button inputs, and pin 8 is used as a scan pulse output. That is, IOB0 thru IOB3 are at H level and IC41 is open.

Table 13-11

PORT	BIT	I/O	CONNECTOR PIN No.	SIGNAL WHEN JOYSTICK IS USED
A	0	Input	PIN1 *1	FWD1
			PIN1 *2	FWD2
	1		PIN2 *1	BACK1
			PIN2 *2	BACK2
	2		PIN3 *1	LEFT1
			PIN3 *2	LEFT2
	3		PIN4 *1	RIGHT1
			PIN4 *2	RIGHT2
	4		PIN5 *1	TRGA1
			PIN5 *2	TRGA2
	5		PIN6 *1	TRGB1
			PIN6 *2	TRGB2
	6		Not used (H)	
	7		CSAR (Cassette tape read data)	
B	0	Output	PIN6 *3	H level
	1		PIN7 *3	H level
	2		PIN6 *3	H level
	3		PIN7 *3	H level
	4		PIN8	
	5		PIN8	
	6		Port A input selection	
	7		Not used (NC)	

*1 Enabled when port B bit 6 is at L level. Connected to controller 1

*2 Enabled when port B bit 6 is at H level. Connected to controller 2

*3 H level when not used as output port. Output via open collector buffer

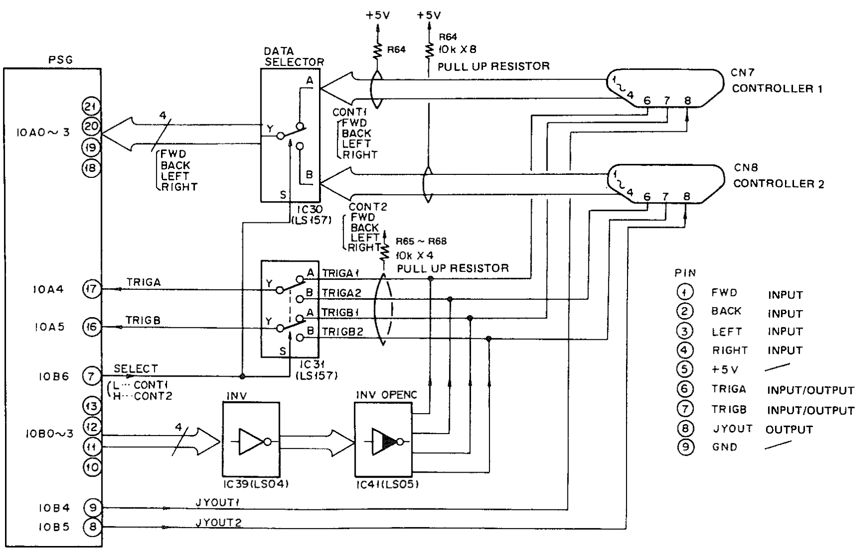


Fig. 13-37 Joystick interface circuit

13. 8. 2 Sound Mixing Circuit

The PSG analog signal outputs A, B, and C are mixed and distributed (A to center, B to left channel, and C to right channel) at a constant power ratio to obtain a two channel output (ASCL and ASCR) with balanced sound pressure level.

Since the PSG analog output stage more or less constitutes a current source, the outputs are converted to voltage levels by external shunt resistances R93 thru R95 before being applied to a mixing amplifier consisting of the Q10 and Q11 amplifiers. The mixing ratios are set so that the A output assures center localization at a ratio of $1/\sqrt{2}$ in respect to the B and C outputs (this setting involves the resistances R79 thru R82 for constant power ratio). In the same way, the PPI (IC4) PC port bit 7 output (SOUND) is mixed and localized centrally via C56, R77, and R78, and the sound input (SUNDIN) from the cartridge slot is mixed and localized via R15, R16, R96, C64, C63, R91, and R92. Thus the audio sound outputs ASCL and ASCR are formed, and passed to the analog ass'y via pins 4 and 2 of J100.

The ASCL and ASCR signals applied to the analog ass'y are passed via a low-pass filter and VR108 where the mixing level is adjusted before the signals are applied to the mixing amplifier (see Fig. 13-41). The signals mixed with input signals from AUDIO IN in the mixing amplifier are subsequently amplified by a power amplifier stage before being passed to built-in speakers or headphones. The levels at each point are as indicated in the level diagram in page 77.

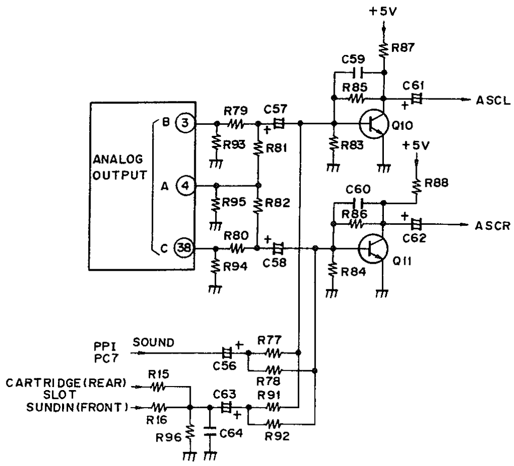


Fig. 13-38 Sound mixing circuit

13.9 PRINTER I/F

Data bus latch data from the 8-bit latch 74LS374 (IC32) is passed to the printer in parallel via pins 2 thru 9. And the $\overline{PSTB}$ signal from the gate array (IC3) is passed as a strobe signal via the IC38 and IC40 buffers to pin 1. The BUSY signal from the printer is passed from pin 11 to the CPU via a three-state buffer (IC45) and data bus D1.

(1) 90H (image 92, 94, and 96H) and 91H (image 91, 93, and 97H) are generated in the gate array by LPT(90 thru 97H) and A0/$\overline{A0}$.

(2) $\overline{90W}$ is formed with 90H WR, and D0 is latched and passed to $\overline{PSTB}$ at the leading edge of $\overline{WR}$, thereby obtaining $\overline{PSTB}$ via the IC38 and IC40 buffers. (IC40 is connected in parallel for fan-out enlargement.)

(3) 90R = $\overline{BUSYEN}$ is formed with 90H RD to enable the BUSY input three-state buffer and input of the BUSY signal to D1.

(4) $\overline{91W}$ = LPTE is formed with 91H WR, and D0 thru D7 are latched at the leading edge of $\overline{WR}$ to obtain the PDB0 thru PDB7 outputs. With the Q output switched to high impedance by the system reset period $\overline{OC}$ changed to H, IC32 prevents occurrence of abnormal operations.

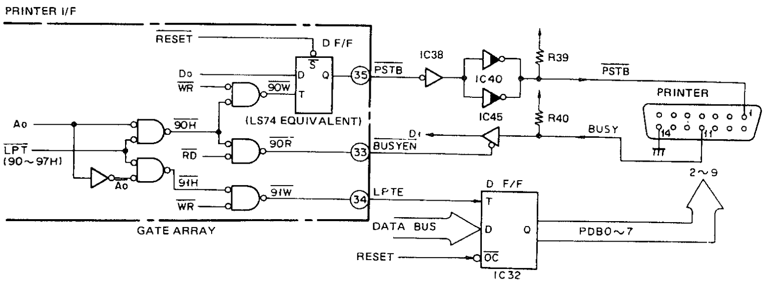


Fig. 13-39 Printer I/F circuit

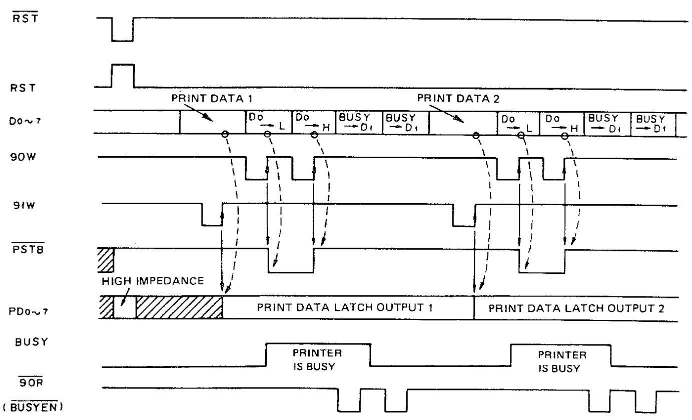


Fig. 13-40 Printer I/F timing chart

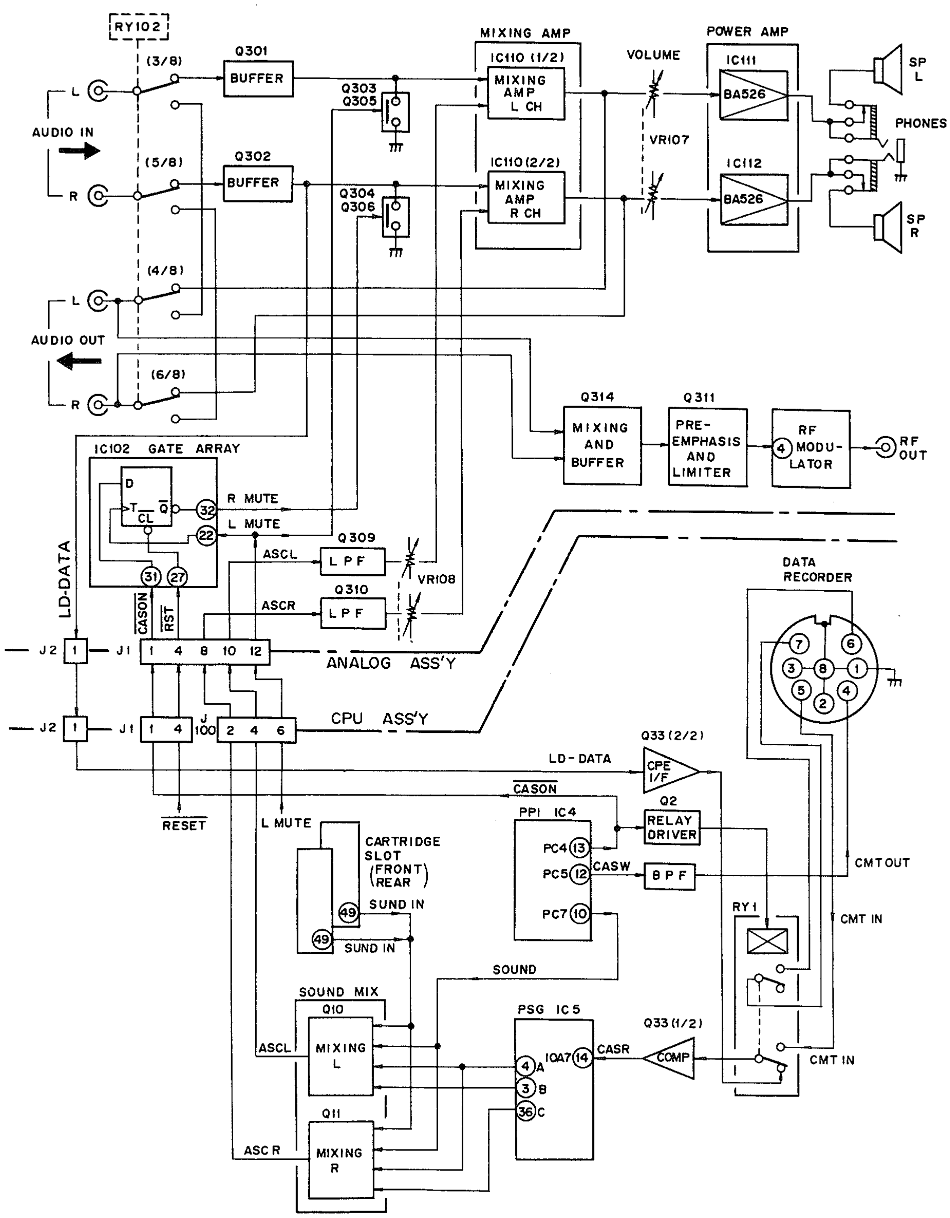


Fig. 13-41 Audio system block diagram

13. 10 KEYBOARD UNIT

The keyboard circuit diagram is outlined in Fig. 13-43. See Section 13.7.3 for a description of exchanges between the keyboard and CPU ass'y.

The key layout in this keyboard is shown in page 16 and 17. The keys are connected to a matrix consisting of Y0 thru Y9 and X0 thru X9 (see Fig. 13-43). The character codes for the PX-7 are listed in TAble 13-12. Note that codes not are listed in Table 13-12. Note that codes not indicated on the keyboard have also been defined. These characters are keyed in by combined use of the SHIFT, GRAPH, and CODE keys as indicated in Fig. 4-43. And when the CAPS LOCK key is pressed, and indicator on the left hand side lights up to indicate that the same characters keyed in by combined use of the SHIFT key can be keyed in. This "shift" mode is switched on or off (indicated by the lamp being switched on or off) each time the CAPS LOCK key is pressed. The [ ]key (called the dead key) includes the following functions.

Table 13-12 Dead key displays

Mode	Function	
normal	grave accent	(`)
normal shift	acute accent	(´)
graph	grave accent	(`)
graph shift	acute accent	(´)
code	circumflex	(^)
code shift	umlaut	(¨)

The above operations are handled by MSX-BASIC software. When the SHIFT key is used together with the GRAPH or CODE key as indicated in the above table, three keys must be pressed together. Consider an example where the SHIFT, GRAPH, and [0] keys are pressed together. Current Ia is passed via R8 in response to the scan pulse from Y0, resulting in X0 being changed to L level to acknowledge that the [0] key has been pressed. If the D1 diode was not included in the circuit shown in Fig. 13-42, however, an image current ib would be passed via R6, D3, and the GRAPH, SHIFT, and [0] keys, resulting in X2 also being changed to L level to infer that the [2] key had also been pressed. Therefore, diodes D1 thru D3 are inserted in the SHIFT, GRAPH, and CODE lines to block reverse currents, and thereby prevent the generation of image keys.

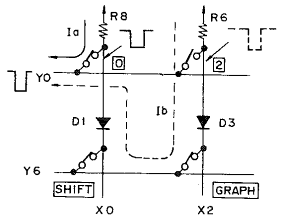


Fig. 13-42 Image key prevention

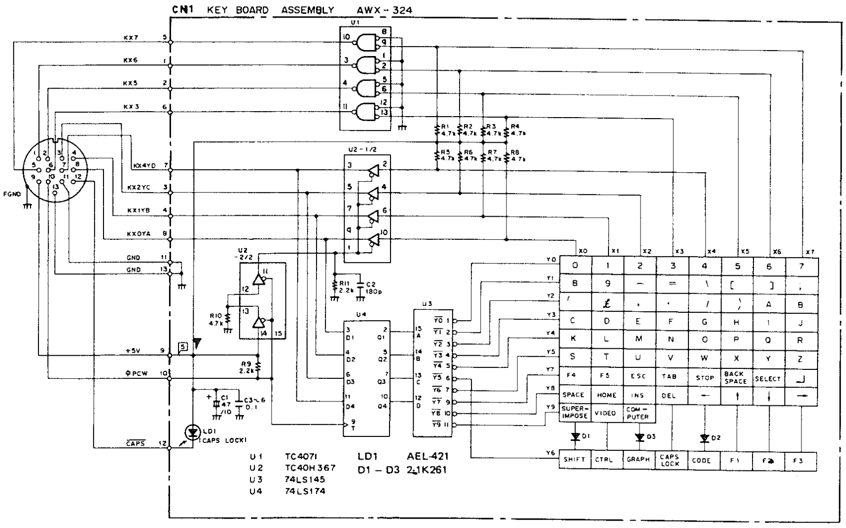
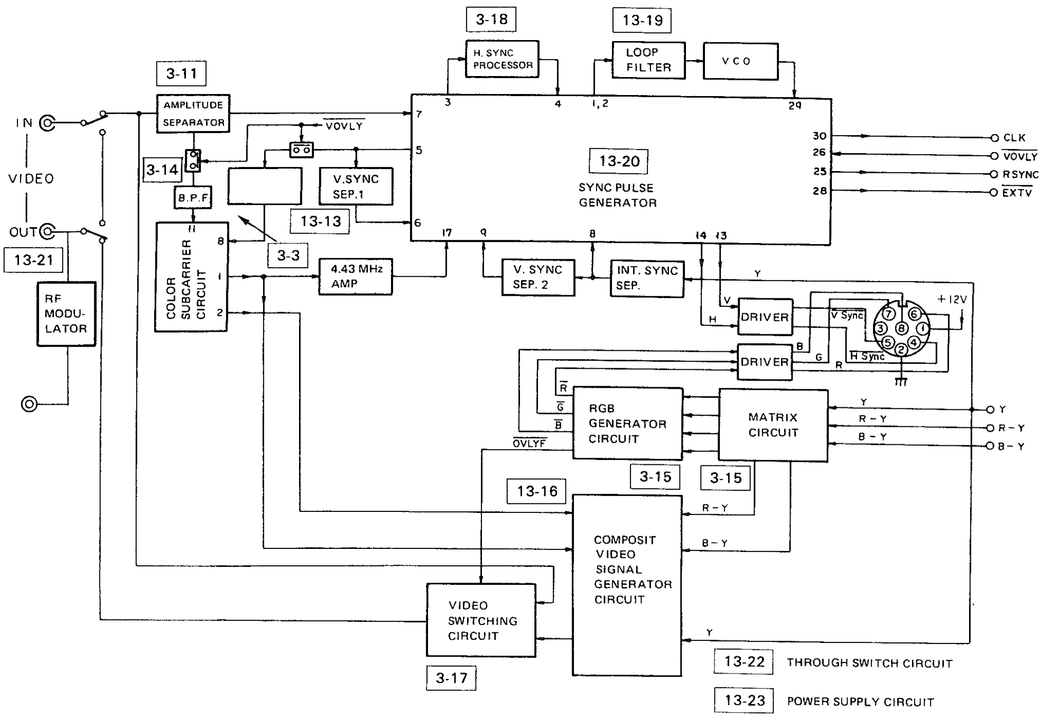


Fig. 13-43 Keyboard circuit diagram



- **VIDEO SIGNAL**

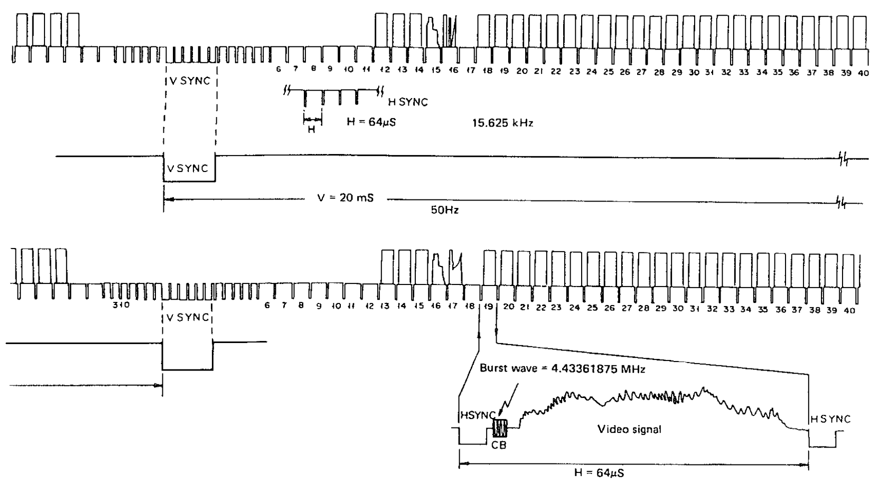


Fig. 13-44 Video signal

13. 11 CIRCUITS USED IN SEPARATE BLOCKS (ANALOG ASS'Y)

13. 11 Synchronizing Signal (Internal) Separator

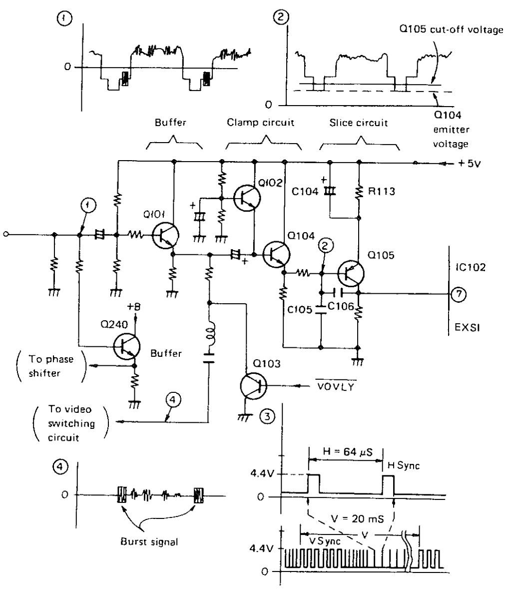
Horizontal and vertical synchronizing pulses are separated as a composite synchronizing signal from the VDP (TMS9129) Y signal (luminance signal).

13. 12 Synchronizing Signal (External) Separator

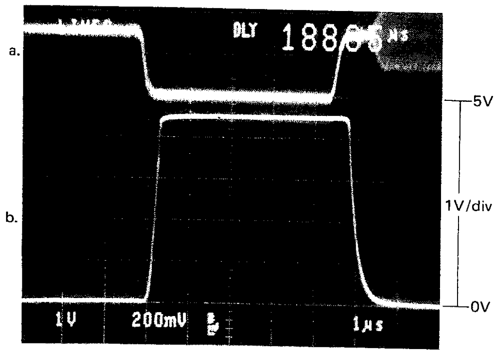
The circuit structure of both the external and internal synchronizing signal separators is practically identical. Therefore, the description here is limited to the external circuit (see Fig. 13-45).

The video signal passed via the Q101 buffer is applied to the Q104 buffer to be added to the DC level of the Q104 base (kept at a constant voltage by the Q102 bias circuit).

The Q105 emitter voltage, on the other hand, is kept at a voltage approximately 0.6V (junction voltage) higher than the Q104 emitter voltage when there is no signal. And since the time constant determined by the Q105 emitter resistance R113 and capacitor C104 is sufficiently large enough, Q105 is turned off when the Q104 emitter voltage exceeds the Q105 cut-off voltage, resulting in the Q105 collector output being changed to L level.



• Horizontal synchronization 1 μs/div



a: VIDEO input waveform (200mV/div)
b: Waveform ③ (composits synchronizing signal output) (1V/div)

Photo 13-1

13. 13 Vertical Synchronizing Signal Separator

The circuit structure of both the internal and external vertical synchronizing signal separators is practically identical. Therefore, the description here is limited to the external circuit (see Fig. 13-46).

The composite synchronizing signal obtained from the external video signal (which is wave-shaped and polarity inverted in the gate array IC102) is passed through a low-pass filter (R156, C141, and R158) where the vertical synchronizing signal is separated, wave shaped by Q114, and ored with R SYNC then applied to Q102 again.

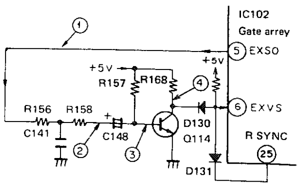


Fig. 13-46 Vertical synchronizing signal separator circuit

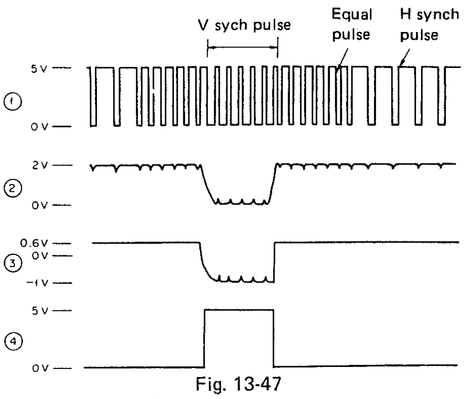


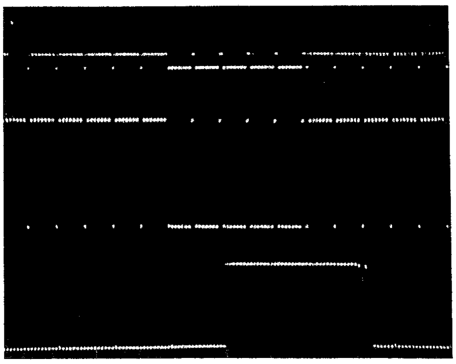
Fig. 13-47

- Horizontal synchronization 50μs/div

a.

b.

c.



a: VIDEO input 500mV/div
b: Waveform (1) (EXSO) 2V/div
c: Waveform (4) (EXVS) 2V/div
Photo 13-2

13. 14 Bandpass Filter, Phase Shifter, and Color Subcarrier Reproduction Circuits

- Bandpass filter (see Fig.13-48)

The bandpass filter is a series connected resonance circuit used to separate the chroma component from external video signals (see Fig. 13-45 wavefrom. ④).

- Phase shifter (see Fig. 13-48)

The purpose of the phase shifter is to combine (in C108 and VR101) the same and opposite phase components of the inverter amplifier Q106, and to shift the phase of the color synchronizing signal (color burst) in the external video signal applied to the color subcarrier reproduction circuit IC101, thereby matching the hue of the computer picture formed at the VIDEO OUT terminal with the hue of the external video signal. The adjustment range of the hue control (VR101) is shown in Fig. 13-49

- Color subcarrier reproduction circuit (see Fig. 13-48)

In addition to the color subcarrier (with 90° phase difference) required by the carrier color signal modulator, the color subcarrier reproduction circuit also generates a reference clock in the synchronizing pulse generator circuit IC102.

Since Q103 is turned off when $\overline{\text{VOVLY}}$ is changed to L level in external video and superimpose modes, the chroma component of the external video signal is passed via the phase shifter to pin 1 of IC101.

The level of this chroma signal is kept constant by the ACC amplifier (amplification to match the input color bar level) by a control voltage from the ACC detector. The output signal appears at pin 4 via a drive circuit (see Photo. 13-3 waveform ⓐ).

Then following a DC level shift at D137 to ensure that the Q107 gate potential does not exceed 5V (IC102 gate array output voltage condition), the IC102 burst gate pulse (BGP2) (see Photo. 13-4 waveform ⓒ) is applied to the gate of Q107, thereby applying only the color burst signal from the chroma signal to the pin 8 input (see Photo. 13-3 waveform ⓑ).

This color burst signal applied to pin 8 is gated again in the burst removing circuit by the burst gate pulse (BGP1) (see Photo. 13-4 waveform ⓓ) on pin 15.

The phase of this gated color burst signal is then compared in a phase comparator with the phase of the color subcarrier oscillator output from the 4.43MHz self-running oscillator, the error voltage being passed via an APC filter (C117, R124, C120, and C118) to control the carrier oscillation phase in generating a color subcarrier synchronized with the color burst of the external video signal.

The carrier vector in the color subcarrier circuit is separated into components which are mutually out of phase by 90° (orthogonal). One of the components serves as the color subcarrier output of the constant phase B-Y axis component, while the other serves as the color subcarrier output of the R-Y axis component where the phase is inverted at each successive line. The B-Y component output is applied to the B-Y demodulator, appearing unchanged at pin 11 due to demodulator balance being upset by R125 and R126. And the R-Y component reflected output is synchronized with the polarity of the external color burst by control pulse from the PAL switch line identifier circuit, resulting in switching of reflected outputs at each line before being applied to the R-Y demodulator input. The final output is obtained from the same pin 10 as the B-Y demodulator output (see Photo. 13-5 thru Photo. 13-7).

In computer mode, the chroma component from the external video signal is muted by Q103 being turned on when $\overline{\text{VOVLY}}$ is changed to H level. The reason for this is to prevent beating between the chroma component generated internally and the external chroma component.

Since the external color burst is not applied to IC101, the color subcarrier oscillator oscillates at the free-running frequency (4.433618MHz), resulting in output of color subcarrier signals (mutually out of phase by 90°) at pins 10 and 11 in the same way as in external and superimpose modes.

And since no color burst is applied to pin 1, on the other hand, the pin 2 voltage exceeds the pin 3 reference voltage, resulting in blanking of the color subcarrier outputs on pins 10 and 11 by the killer detector and killer blanking circuits, thereby forcing a lowering of the voltage on pin 2 by IC102 VOVOUT (L when in computer mode) via R120.

Since the pin 10 and 11 color subcarrier outputs are also in blank (IC101 function) during the pin 7 PAL pulse intervals, enlarging the pulse width will prevent the generation of color bursts in the carrier color signal modulator. Therefore, the width is limited to about 800ns and the pulse position is set near the front porch of the internal/external horizontal synchronizing signal, thereby eliminating the influence of the blanking (see Photo. 13-4 waveform ⓑ).

If the nth line vector of the color subcarrier outputs on pins 10 and 11 are set as indicated in Photo. 13-5 in computer mode, and the PAL pulse on pin 7 is counted up by 1, the vecotr at the (n+1)th line shown in Photo. 13-6 is obtained, and the phase of the color subcarrier of the R-Y axis component is inverted.

Part of the oscillator output from pin 13 of the color subcarrier oscillator is picked up by the reference clock for the synchronizing pulse generator IC102, and is then amplified by Q108 before being applied to pin 17 of IC102.

In addition to controlling the input level of the carrier color signal modulator by Q108 and Q109, the color subcarrier output from pins 10 and 11 of IC101 also inverts the B-Y phase at Q108 to ensure proper polarity for the carrier color signal.

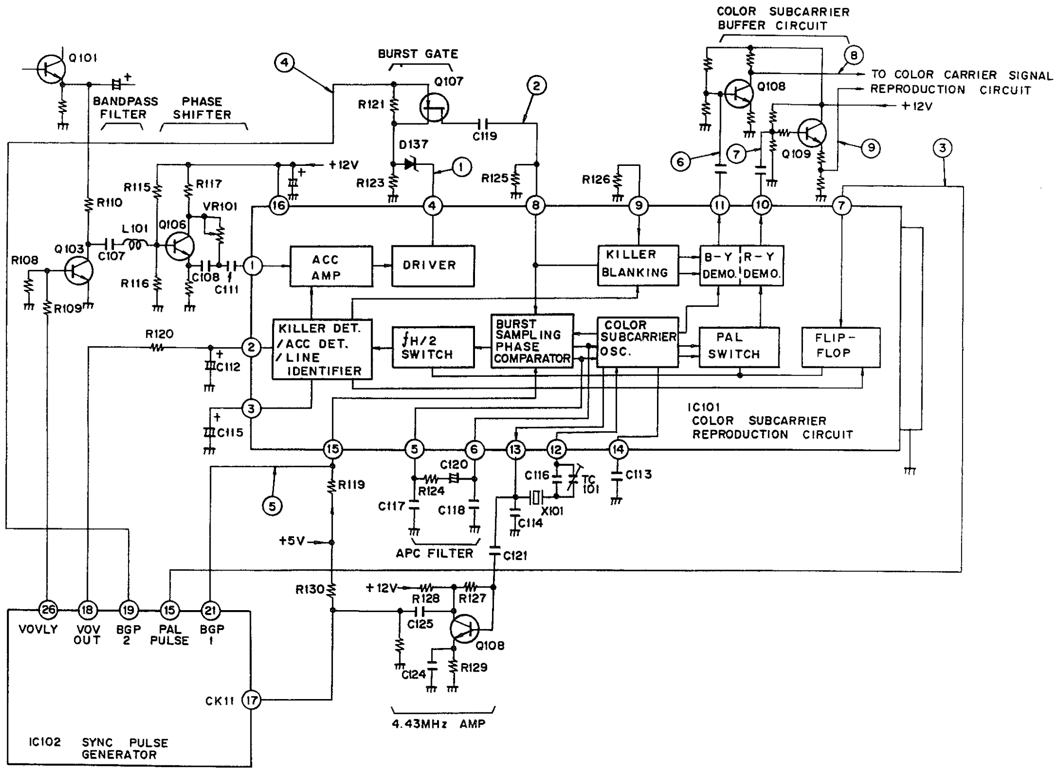


Fig. 13-48 Color Subcarrier reproduction circuit

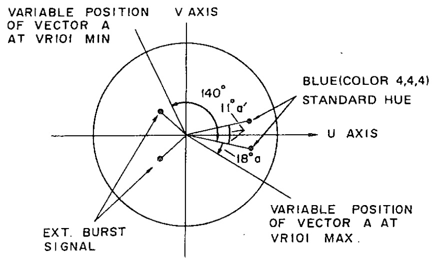


Fig. 13-49 Hue changes at VIDEO OUT (Synthesis mode only)

a. IC101 PIN 4
(2V/div)

b. IC101 PIN 8
(1V/div)

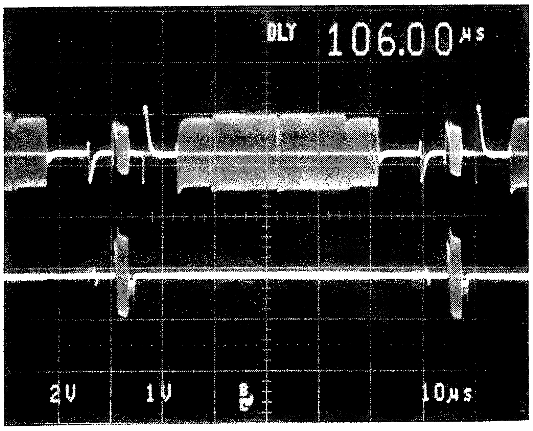


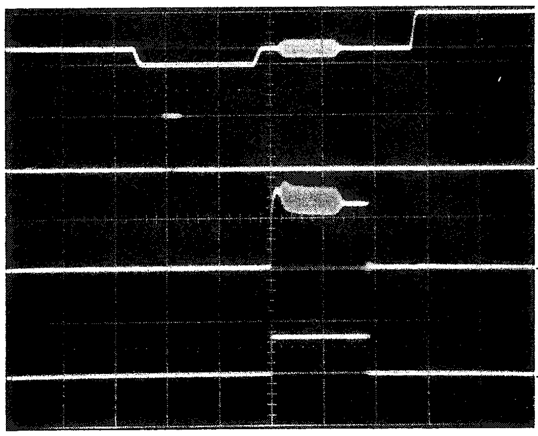
Photo 13-3 Color burst sampling

a. EXTERNAL
VIDEO
INPUT

b. IC101 PIN 7
PAL PULSE
(5V/div)

c. Q107 GATE
BGP2
(2V/div)

d. IC101 PIN 15
BGP1
(2V/div)



—0V
—0V
—0V

Photo 13-4 VIDEO IN, PAL PULSE, BGP2 and BGP1 timing

⑧ / ⑨ outputs
(Q108 and Q109 outputs)

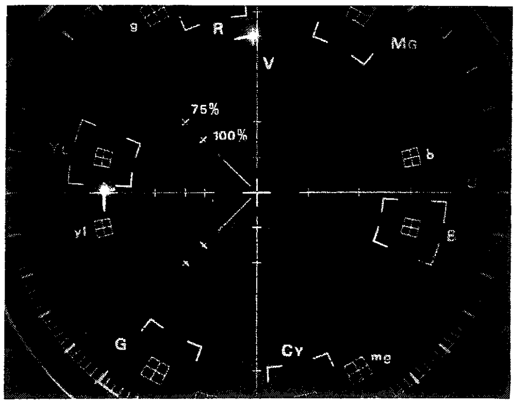


Photo 13-5 Reproduced color subcarrier vector (nth line)

⑧ / ⑨ outputs
(Q108 and Q109 outputs)

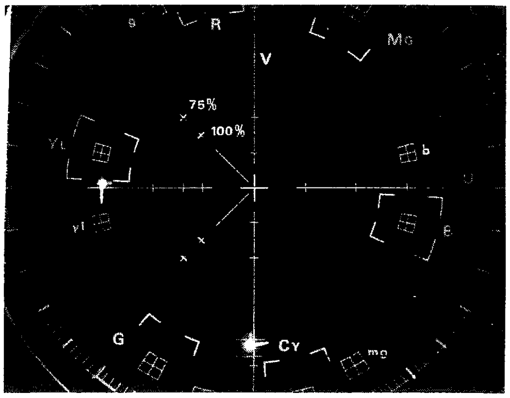


Photo 13-6 Reproduced color subcarrier vector (n+1) th line

a. ⑥ waveform B-Y axis synthesized color subcarrier output (IC101 pin 11)

b. ⑦ waveform R-Y axis synthesized color subcarrier output (IC101 pin 10)

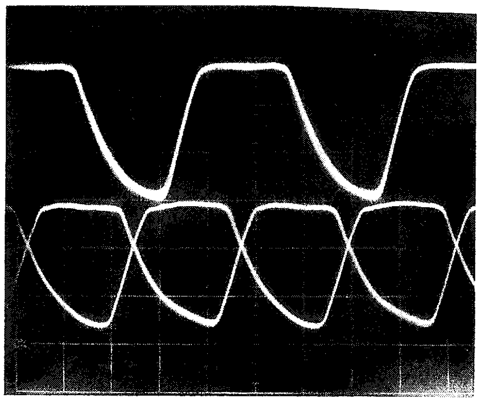


Photo 13-7 Reproduced color subcarrier outputs

13. 15 Matrix Circuit

- RB Generator Circuit and Matrix (see Fig. 13-50)

The video signal output from the computer consists of Y (luminance signal), R-Y (red/luminance difference signal) and B-Y (blue/luminance difference signal) components from the VDP (TMS9129).

The RGB mixing ratio in each signal is decided by the following equations (1), (2), and (3), the RB signal being obtained by adding the R-Y and Y, and B-Y and Y signals on a 1:1 basis.

(1) Y = 0.30R + 0.59G + 0.11B
(2) R-Y = 0.70R − 0.59G − 0.11B R → R
(3) B-Y = −0.30R − 0.59G + 0.89B B → B

The R signal is obtained by adding Y and R-Y on a 1:1 basis in R210/R205 before being applied to pin 5 of IC105, and the B signal is obtained by adding Y and B-Y on a 1:1 basis in R209/R204 before being applied to pin 3 of IC105. These signals are then compared with the L level on VR104, and are obtained as respective negative outputs from pins 1 and 7 of IC105. The negative R and B signals are subsequently inverted in the inverted output buffer IC106 to obtain positive R and B signals from the RGB OUTPUT pins 6 and 8 (see Photo. 13-8 and Photo. 13-9).

- G and $\overline{\text{OVLYF}}$ Generator Circuit (see Fig. 13-50)

The G and $\overline{\text{OVLYF}}$ signals are obtained from the three Y, R-Y, and B-Y outputs from the VDP (TMS9129) described above. The G signal is obtained by addition to the other signals in accordance with the following equation.

(4) G = Y − [0.51(R-Y) + 0.19(B-Y)]

The 0.51(R-Y) + 0.19(B-Y) addition is executed by R207/R208, and the inverted signal is formed by Q205/Q206. The Y signal is added by R215/R216, the result being added to pin 3 of IC104 and the output being obtained from pin 1. The G output is then inverted by the output inverter buffer IC106 to become the positive polarity G signal which is obtained from the pin 7 RGB OUTPUT terminal (see Photo. 13-10).

- $\overline{\text{OVLYF}}$

The overlay flag is included in the R-Y and B-Y output signals during VDP (TMS9129) external synchronizing mode (SUPERIMPOSE, VIDEO), and in the PX-7, $\overline{\text{OVLYF}}$ is obtained from the B-Y signal. Since $\overline{\text{OVLYF}}$ is used at the same comparator level as the G signal, the B-Y signal is subject to a positive voltage shift (since the flag is included as a negative signal in the color difference signal) before being applied to pin 5 of IC104 to obtain the $\overline{\text{OVLYF}}$ signal (see Photo. 13-11 and and Photo. 13-12).

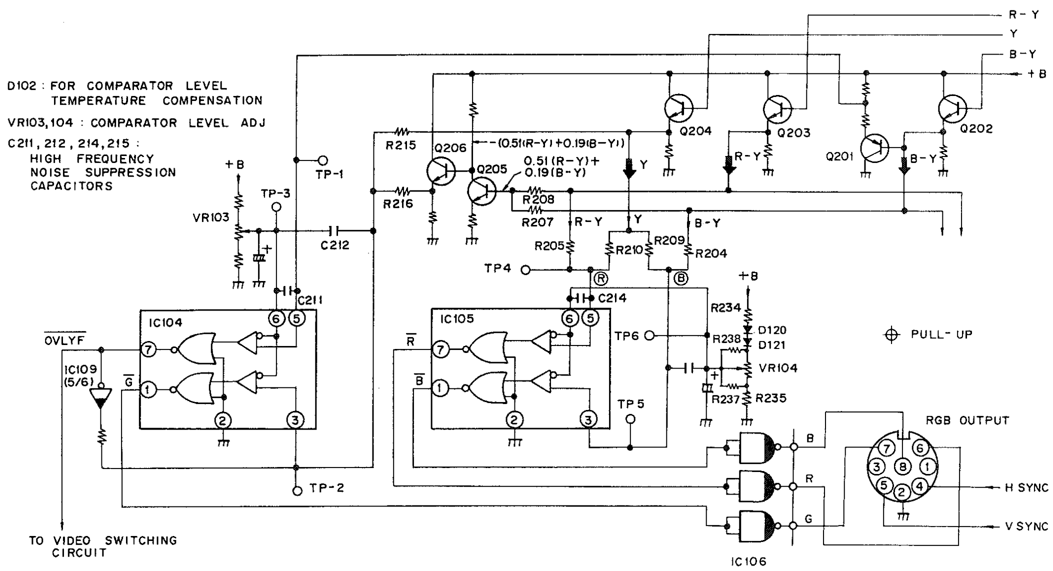


Fig. 13-50 Matrix and RGB generator circuits

On the other hand, since the overlay flag is included in the color difference signal, a correct RGB signal (analog signal) cannot be obtained from the matrix circuit described earlier during external synchronization mode. Although this has no effect on the potential obtained when switching to TTL level where the R and B signals are concerned, a signal which appears to include the G signal is obtained if a flag is present when the G signal is concerned. Hence, to prevent the generation of a G signal in the external signal section, the G output is blocked while $\overline{OVLYF}$ is at H level (that is, while the external video signal is displayed) as a result of $\overline{OVLYF}$ being inverted and added to the analog signal (pin 3 of IC104) (see Fig. 13-51).

The OVLYF signal exists in the following states.

Table 13-13

Mode	$\overline{OVLYF}$	
Superimpose mode	External video signal display section	H
	Computer vide signal section	L
External video mode	Always H	
Computer mode	Always L	

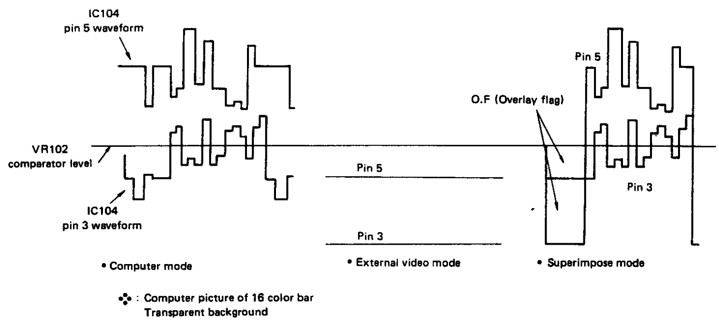
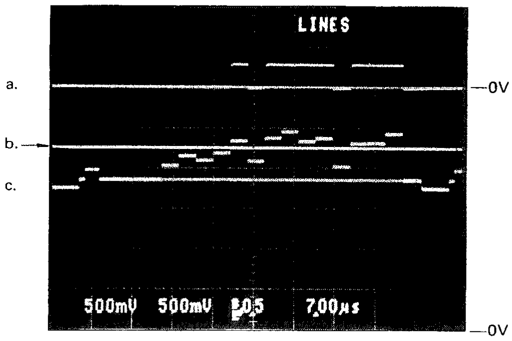
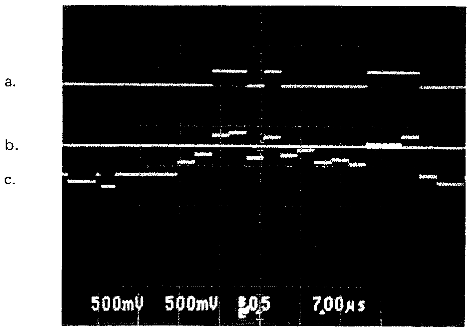


Fig. 13-51 Waveforms at pins 3 and 5 of IC104 during each



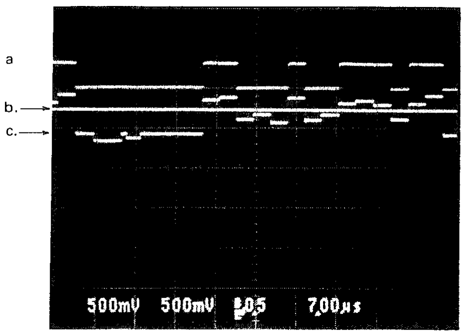
a: RGB OUTPUT (R OUTPUT) 5V/div
(when RGB pack inserted)
b: TP-6 (VR104 comparator reference voltage) 500mV/div
c: TP-4 500mV/div

Photo. 13-8 16 color bar RGB generator circuit waveforms



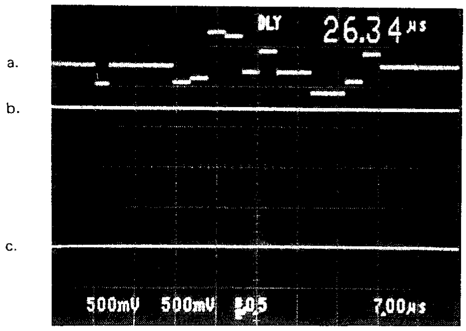
a: RGB OUTPUT (B OUTPUT) 5V/div (When RGB pack inserted)
b: TP-6 (VR104 comparator reference voltage) 500mV/div
c: TP-5 500mV/div

Photo. 13-9



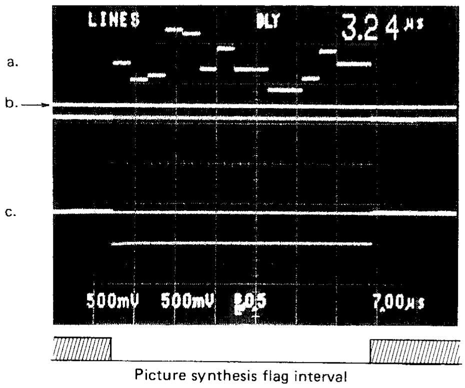
a: RGB OUTPUT (G OUTPUT) 5V/div (When RGB pack inserted)
b: TP-3 (VR103 comparator reference voltage) 500mV/div
c: TP-2 500mV/div

Photo. 13-10



a: TP-1 (DC shift B-Y signal) 500mV/div
b: TP-3 (VR103 comparator reference voltage) 500mV/div
c: IC104 PIN 7 (OVLYF signal) 5V/div

Photo 13-11 OVLYF in computer mode



a: TP-1 (DC shift B-Y signal) 500mV/div
b: TP-3 (VR103 comparator reference voltage) 500mV/div
c: IC104 PIN 7 (OVLYF signal) 5V/div

Photo. 13-12 $\overline{\text{OVLYF}}$ in picture synthesis mode

13. 16 Composite Video Signal Generator Circuit (see Fig. 13-52)

The two color subcarriers (4.433618MHz) generated in the color subcarrier reproduction circuit, and which are at a mutual phase difference of 90°undergo balanced modulation by the R-Y and B-Y signals in the composite video signal generator circuit, and the carrier color signal is combined with the Y signal.

- Carrier color signal modulator/overlay eliminator/bias stabilizer circuit

Since the IC107 pin 4 and 6 inputs are DC coupled with the R-Y and B-Y signals, the DC level will vary due to variations in the VDP and buffers. For this reason, the bias voltage applied to IC107 can be varied by VR106 (carrier suppression adjustment control) to ensure that IC107 (balanced modulator) is properly balanced. The outputs from pins 1 and 9 are mixed by R269/R270 for carrier color signal modulated by IC107 to obtain the X part of the PAL system composite video signal in equation (1). (See Photo. 13-19 and Photo. 13-20.)
Equation (1)

PAL composite video signal

$$= Y + (B-Y)/2.03 \, \cos \omega sct \pm (R-Y)/1.14 \, \sin \omega sct$$

$$= Y \underbrace{+ 0.49(B-Y) \cos \omega sct \pm 0.88(R-Y) \sin \omega sct}_{\text{X part}}$$

The matrix circuit R-Y and B-Y Q203/Q202 buffer outputs appear as shown in Photo. 13-13 (computer mode) and Photo. 13-14 (synthesis mode). In synthesis mode the picture synthesis flag

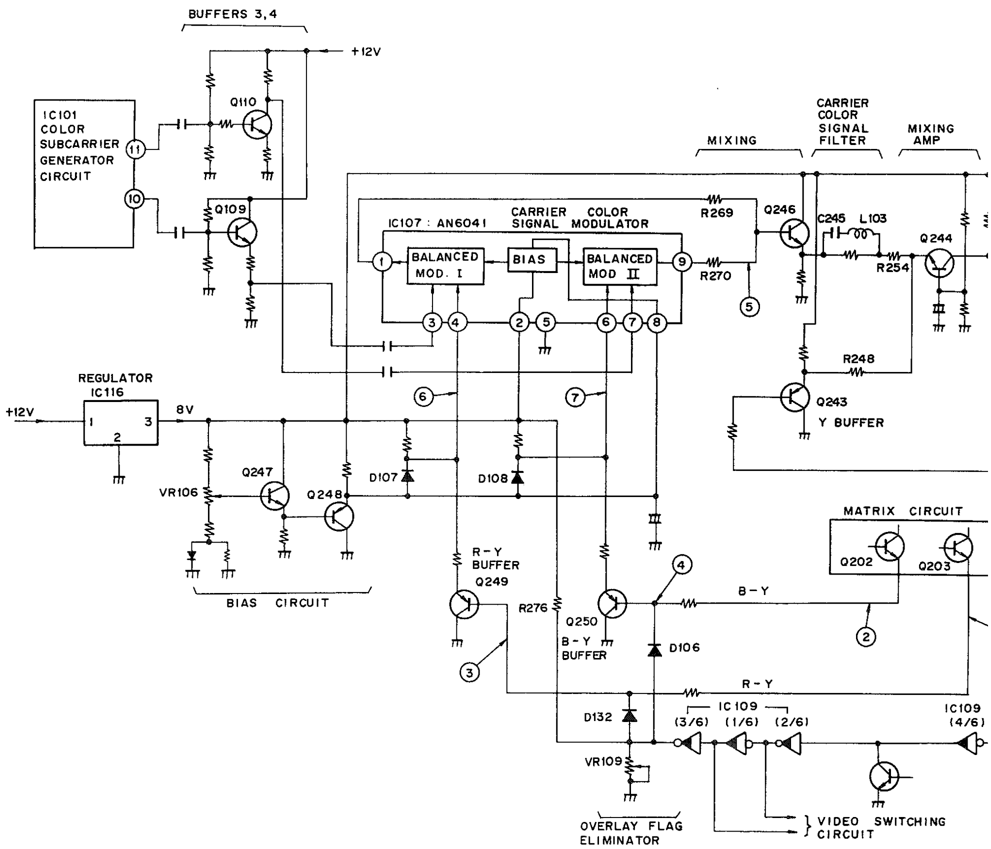
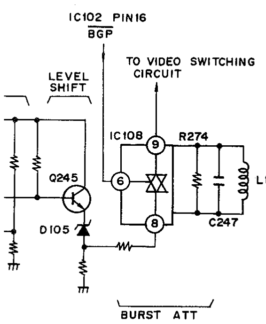


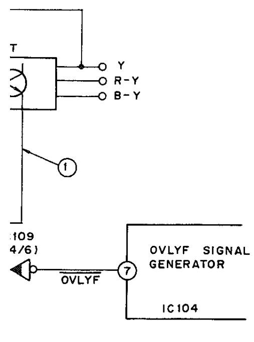
Fig. 13-52 Composite video signal generator

is included in the color difference signal where the voltage is lower than the achromatic level. If this signal is then modulated by the color signal, there will be a considerable increase in color subcarrier leak at this section, resulting in a delay when passed through the carrier color signal filter, and the generation of a spike during external/internal switching (see Photo. 13-17) at the video output terminal. Characters are thus colored green in this case.

To improve this situation, the R-Y and B-Y signals are limited by D106 and D132 to the achromatic level when OVLYF is H (external video display section). VR109 (white adjustment control) is the control used to adjust the achromatic level.

The Q249 and Q250 base waveforms during computer and synthesis modes are shown in Photo. 13-15 and Photo. 13-16. Photo. 13-18 shows the improvement on the switching spike achieved by the overlay eliminator circuit.





Q249 and Q250 are level shift transistors (pnp type) for the B-Y and R-Y signals, and are involved in temperature compensation for the junction voltage between the base and emitter due to application of emitter outputs from the matrix circuit Q202 and Q203 (npn type transistors). In the bias circuit, too, temperature compensation involves the use of similar pnp and npn transistors.

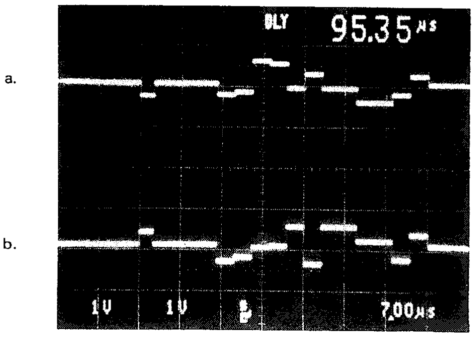
Since regulated power voltage is required by the carrier color signal modulator circuit IC107 and the bias circuit, the voltage is regulated a second time by the triple terminal regulator IC116.

- Carrier color signal filter/mixing amplifier/burst ATT

The carrier color signal output from the carrier color signal modulator is passed via a mixing buffer (Q246) and carrier color signal filter (*) to be added to the Y signal (luminance signal) from the VDP in accordance with the R248/R254 ratio, thereby forming the composite video signal. After being amplified to about 1Vp-p by Q244/Q245, this signal is subject to a level shift of about 5V at D105.

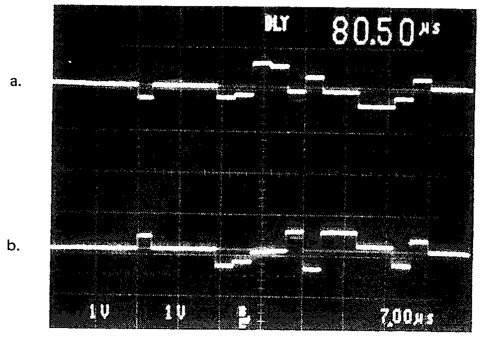
The signal is then passed to the pin 8 input of the analog switching IC (IC108). Since the L104/ C247 series resonance circuit connected to the input and output of this switch resonates at the color subcarrier frequency, only the composite video signal burst is attenuated by R274 when a BGP pulse (burst interval L) is applied to pin 6 (the DC component being bypassed by L104 without any level shift). The burst level in the composite video signal is thus matched with standard signal value during computer mode. (*The carrier color signal filter is a band limiting bandpass filter used to minimize dot interference.)

● **16 COLOR BAR DISPLAY**



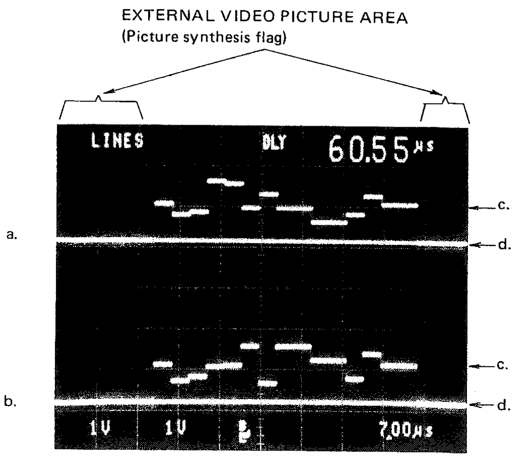
a: WAVEFORM ② B-Y 1V/div
b: WAVEFORM ① R-Y 1V/div

Photo. 13-13 Computer mode



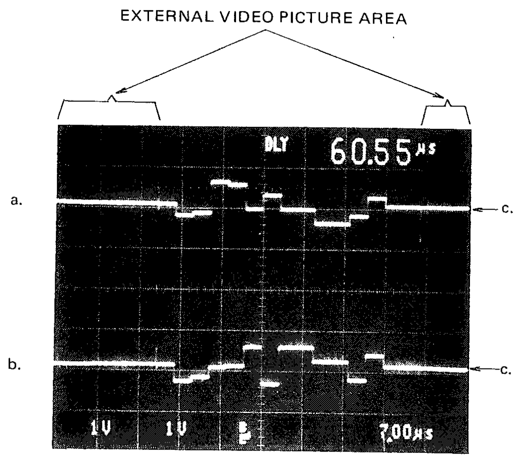
a: WAVEFORM ④ B-Y 1V/div
b: WAVEFORM ③ R-Y 1V/div

Photo 13-15 Computer mode



a: WAVEFORM ② B-Y 1V/div
b: WAVEFORM ① R-Y 1V/div
c: ACHROMATIC LEVEL
d: PICTURE SYNTHESIS FLAG LEVEL

Photo. 13-14 Synthesis mode

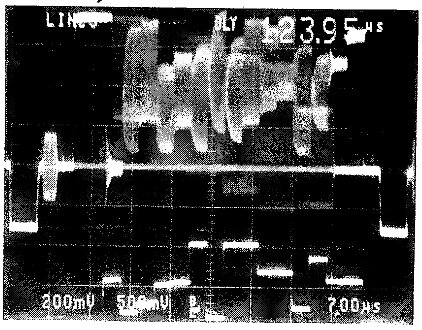


a: WAVEFORM ② B-Y 1V/div
b: WAVEFORM ① R-Y 1V/div
c: ACHROMATIC LEVEL

Photo. 13-16 Synthesis mode

SWITCHING SPIKE

a.

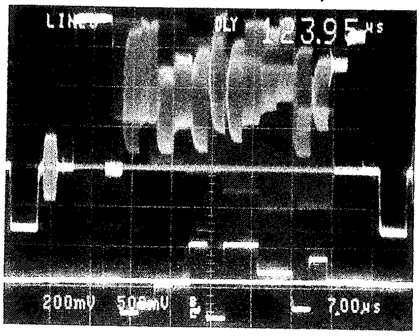


b.

a: VIDEO OUT terminal output
[External: white 100% puls internal 16 color bar]
(75-ohm load) (200mV/div)
b: ③ (R-Y input) waveform (500mV/div)

Photo. 13-17 Without overlay flag eliminator

a.

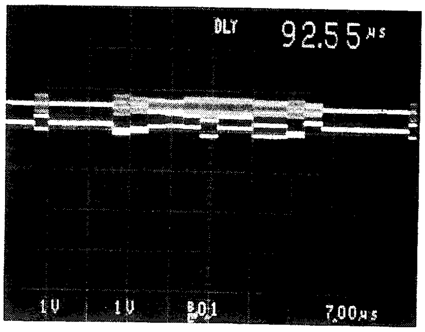


b.

a: VIDEO OUT terminal output
[External: white 100% puls internal 16 color bar]
(75=ohm load) (200mV/div)
b: ③ (R-Y input) waveform (500mV/div)

Photo. 13-18 With overlay flag eliminator

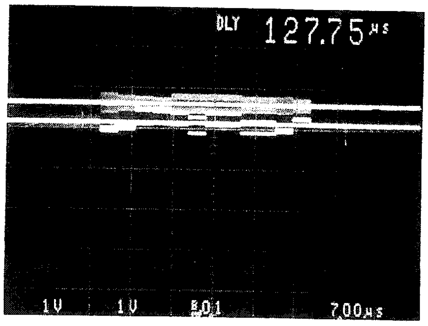
a.
b.



a: Carrier color signal 1V/div
b: (R-Y signal) 1V/div
(B-Y signal) 1V/div

Photo. 13-19 Computer mode (16 color bar)

a.
b.



a: CARRIER COLOR SIGNAL 1V/div
b: (R-Y SIGNAL) 1V/div
(B-Y SIGNAL) 1V/div

Photo. 13-20 Synthesis mode (16 color bar)

13. 17 Video Switching Circuit (see Fig. 13-53)

- Buffer 2 and clamp circuit 1

To match the pedestal level of the computer picture signal processed by DC coupling (the level at point ① in Fig. 13-53) with the pedestal level of an external video signal, the DC level (determined by the Q241/Q242 clamp circuit) of that external video signal is adjusted by a video level adjustment control (VR105) after the signal has been passed through the Q240 buffer (the adjusted level being the level at point ② in Fig. 13-53 (see Photo. 13-21).

D103 and D104 are used in temperature compensation of the Q241/Q242 junction voltage.

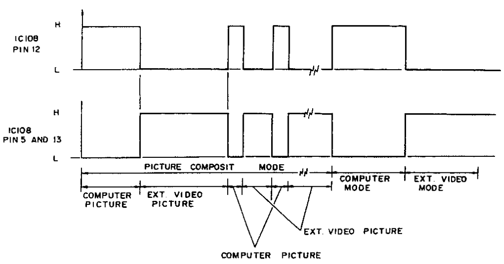
- Video switching circuit

This circuit switches the external video signal and computer signal outputs in response to the OVLYF signal from pin 7 of IC104.

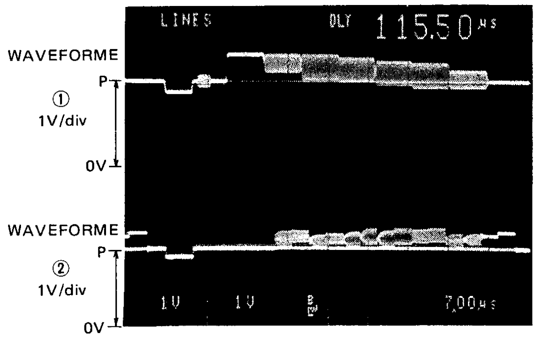
When OVLYF is H, pins 5 and 13 of analog switch IC108 are also changed to H to select the external video signal. And when OVLYF is L, pin 12 of IC108 is changed to H to select the computer signal, the output signal being obtained from pin 11 of IC108.

- Video amplifier

The video amplifier (Q282/Q281/Q280) is a current input type of amplifier which amplifies the signal switched from the video switching circuit to obtain a 2Vp-p output at the VIDEO OUT terminal via R280 (see Fig. 13-53).



- Video switching control signals



P: PEDESTAL LEVEL

Photo. 13-21 External/internal video signal levels (Pincture synthesis mode) (color bar (external) (16 color bar (internal)

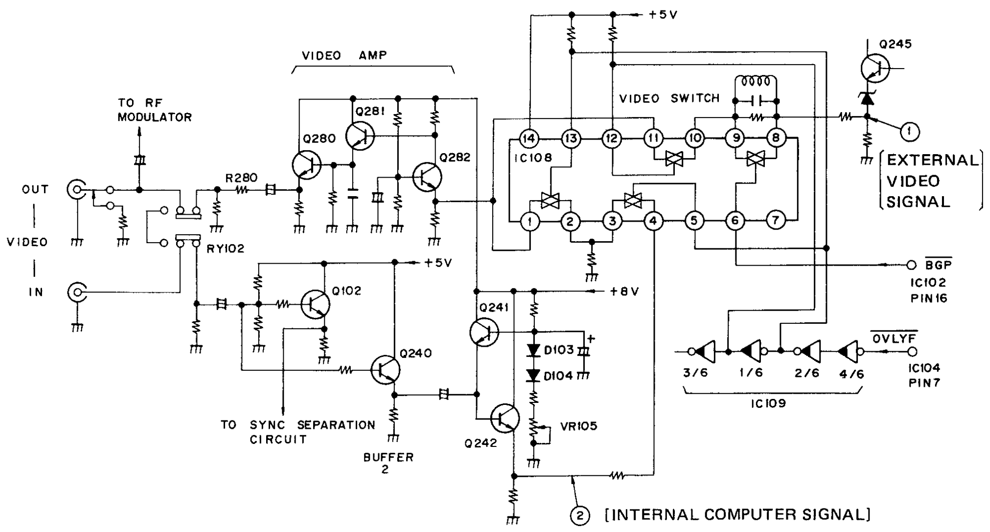


Fig. 13-53 Video switching circuit

13. 18 Horizontal Synchronizing Signal Processing Circuit (see Fig. 13-54)

The horizontal synchronizing signal processing circuit generates a 15.625kHz horizontal synchronizing signal frequency synchronized with the external video signal and VDP Y signal (luminance signal) on the basis of the horizontal synchronizing signal separated from those signals.

IC103 forms a PLL oscillator which oscillates at the free-running frequency when there is no input applied. Although this free-running frequency can be adjusted by VR102, the PLL will not lock if the frequency is too far away from 15.625kHz.

The horizontal position can be adjusted to a small degree by VR102 within the range where the PLL is locked (see Photo. 13-22). The C150 and C151 mylar capacitors are used for temperature compensation for the ocillating frequency (see Photo. 13-22).

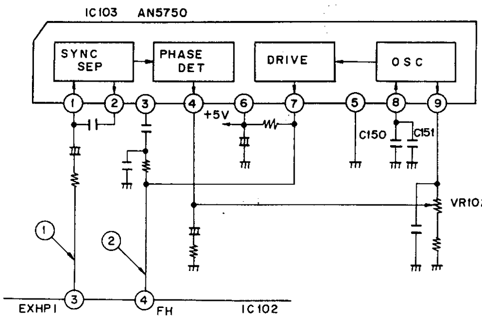
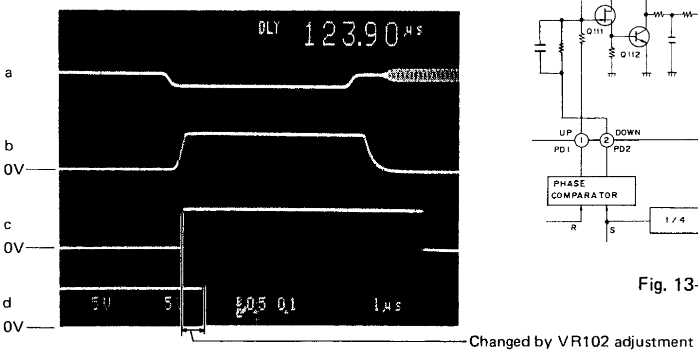


Fig. 13-54 Horizontal synchronizing signal processing circuit



a: External video input (horizontal synchronizing signal)
b: External composite synchronizing signal input (IC102 pin 7 EXSI) 5V/div.
c: Waveform ① EXHP1 5V/div.
d: Waveform ② FH 5V/div.

Photo. 13-22 Video input/EXSI/EXHPI/FH timing (picture synthesis mode)

13. 19 Loop Filter and VCO (see Fig. 13-55)

This loop filter and VCO (voltage controlled oscillator) form a PLL oscillator with the phase comparator and counter gate array (synchronizing pulse generator) IC102. A 10.6MHz clock for the VDP (TMS9129) is generated.

The error voltage from the gate array phase comparator (comparison frequency of 3.90625kHz in synthesis mode and 3.903kHz in computer mode) is passed to the Q111/Q112 loop filter. The filter output is then applied to the D101 variable capacitance diode to control the VCO. The VCO oscillates on the basis of the 4.433618MHz color subcarrier signal during computer mode, and on the basis of the frequency of the horizontal synchronizing signal in the external video signal when in external video mode, the oscillating frequency being locked at frequencies determined by the following equations:—

- When in computer mode
  f_{CLK} = 4.433618MHz (color subcarrier frequency) /1136 x 4 x 684 = 10.67815039MHz

- When in video picture synthesis mode
  f_{CLK} = 15.625kHz (external video horizontal synchronizing signal frequency) x 684 = 10.687500MHz

A DC bias is applied to the gate array via R154 and R153 to ensure that the oscillator output is applied within the 0 to 5V range. The D134 diode protects the gate array from inputs in excess of 5V (see Photo. 13-23).

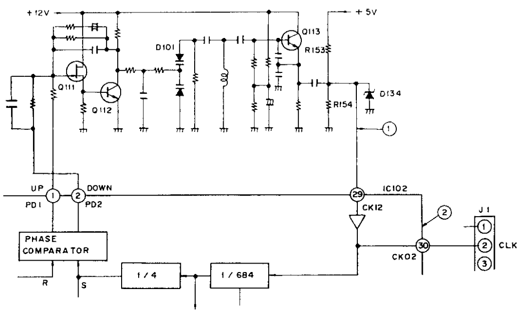


Fig. 13-55 Loop filter and VCO circuit

WAVEFORM
②
2V/div

WAVEFORM
①
2V/div

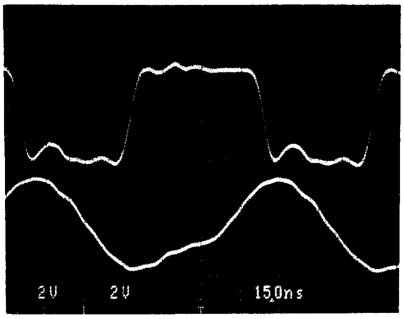


Photo. 13-23 VDP clock waveforms

13. 20 Synchronizing Pulse Generator (Gate Array IC 102)

The synchronizing pulse generator consists of the following component circuits.

(1) External horizontal synchronizing signal noise remover
(2) External video signal detector
(3) VDP clock generator (4) VDP clock generation reference signal generator
(5) Reference signal switching circuit for the horizontal and vertical synchronizing signals plus PLL generator used in picture synthesis
(6) Burst gate pulse generator
(7) PAL pulse generator
(8) Computer sound muting control circuit

Operation of the synchronizing pulse generator differs considerably in computer mode and external video/picture synthesis mode.

- Computer mode

When in computer mode ($\overline{VOVLY}$ = H), the gate array internal connections are as shown in Fig. 13-57. In computer mode, the vertical and composite synchronizing signals separated from the computer picture output signal from the VDP (TMS9129) are applied to the INVS and INHS pins (pins 9 and 8). The output from pin 13 (VSYNC) is inverted by the IC109(6/6) driver and applied as a negative vertical synchronizing signal to the RGB terminal (pin 5). And the composite synchronizing signal from pin 14 (HSYNC) is NORed with the vertical synchronizing signal at the IC106 driver to remove the vertical synchronizing component before being applied as a negative horizontal synchronizing signal to the RGB terminal (pin 4).

The color subcarrier (4.433618MHz) is applied to pin 17 (CKI1) from the color subcarrier oscillator, and divided by 1136 in the frequency divider to obtain a 3.903kHz signal which is applied as a reference signal to the phase comparator. The VCO output (10.67815MHz), on the other hand, is applied to pin 29 (CKI2) where it is rectified by a Schumitt buffer and passed as the VDP clock from pin 30 (CKO2). Part of this output is divided once by 684 and again by 4 (overall division by 2736) to become a 3.903kHz comparator signal to be applied to the phase comparator. The phase comparator output thus forms a loop with the loop filter and VCO which in turn forms a PLL oscillator circuit based on the divided signal obtained from the color subcarrier. A horizontal synchronizing signal obtained by dividing the VDP clock (10.67815MHz) by 684 is combined with a vertical synchronizing signal separated from the external video signal and applied to pin 25 (RSYNC).

When there is no external video signal applied to pin 28 ($\overline{EXTV}$) (that is, no input applied to pin 7 (EXSI)), the counter and FF2 are not reset — the counter is incremented by the output from a frequency halving circuit, and FF2 remains in a triggered state with an H output on pin 28. When an external video signal is then applied, a composite synchronizing signal (external synchronizing signal) is applied to pin 7 (EXSI), and the counter and FF2 are reset by the horizontal synchronizing signal in the input. Pin 28 ($\overline{EXTV}$) is thus changed to L level. However, since the counter divides the 7.806kHz signal (halved horizontal synchronizing signal) by 7, FF2 is inverted if more than 14 pulses (897μS MIN.) have been extracted from the horizontal synchronizing signal from pin 7 (EXSI), and the pin 28 ($\overline{EXTV}$) output is changed to H level. Hence, the pin 28 output serves as a detector signal which is H when no external video signal is applied and L when a signal is applied.

The same HSYNC composite synchronizing signal is also passed from pin 3 (EXHP1). to pin 4 (FH) via the horizontal synchronizing signal processing circuit. This FH is then applied to the PAL pulse generator together with the halved and inverted CKI1, and a PAL pulse output signal which controls the PAL switch with a pulse width of about 450ns and which is triggered by the FH trailing edge is obtained from pin 15 (PAL PULSE). (Delay time: 0 to 450ns). Furthermore, the HSYNC (composite synchronizing signal) obtained from

INHS, and the CKI1 inverted signal passed via the counter are applied to the burst gate generator. The HSYNC is changed to L at the trailing edge, and back to H after counting CKI1 by 17 (pulse width of 3.6 to 3.8μsec), resulting in output of $\overline{BGP}$ from pin 16 for use in burst ATT circuit switching. The same burst gate generator is also used to generate BGP2 and BGP1 outputs for control of the pin 19 / pin 21 open drain output burst sampling circuit.

Relevant waveforms are shown in Photo. 13-24

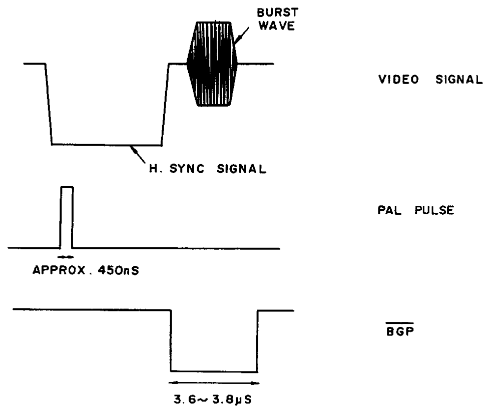


Fig. 13-56 Relevant waveforms in computer mode

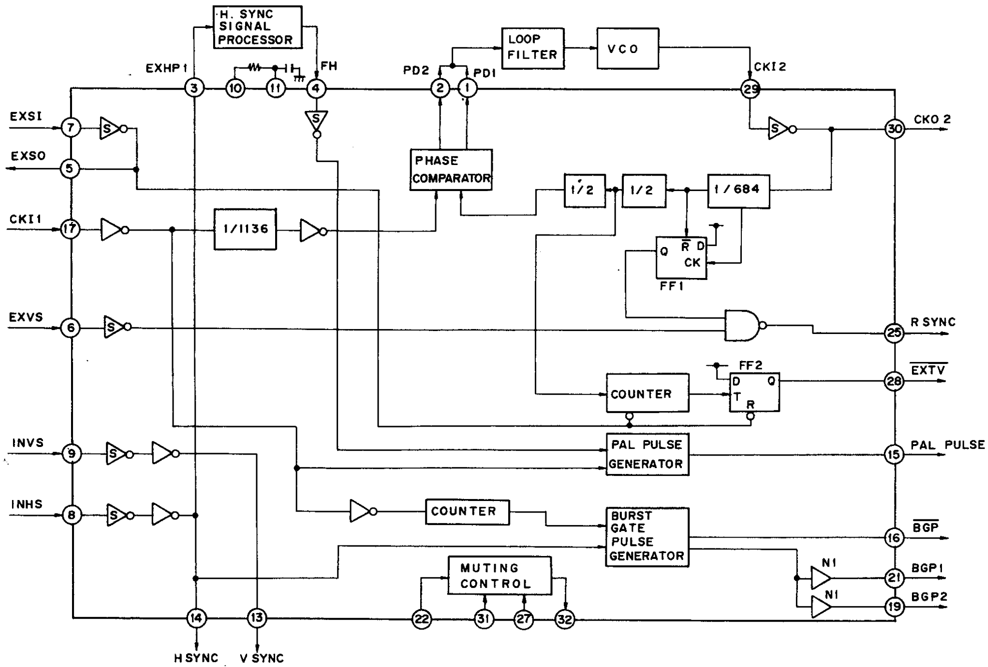
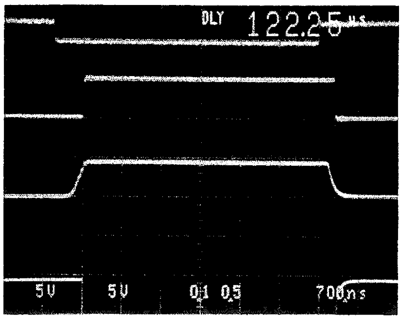
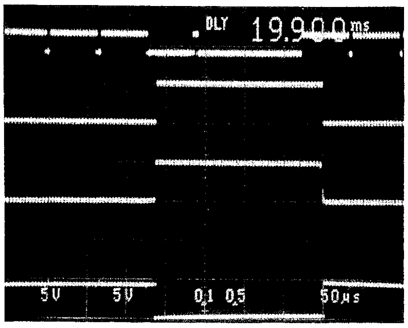


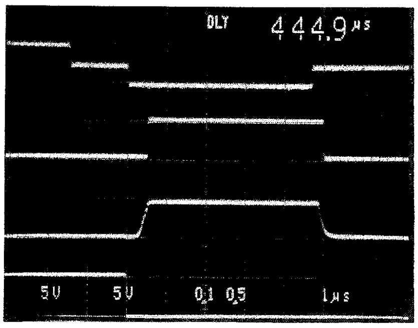
Fig. 13-57 Synchronizing pulse generator
(Computer mode)



(a) H SYNC



(b) V SYNC



(c) FH

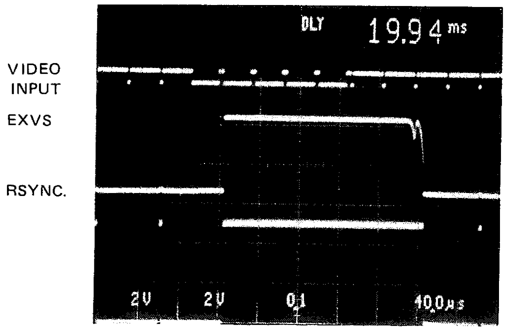
Photo 13-24 Relevant waveforms in computer mode

- External video and superimpose modes

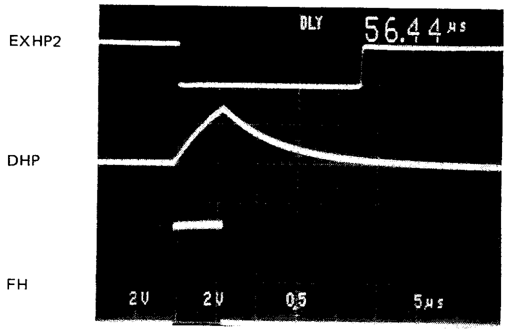
The gate array internal connections in external video and superimpose modes are outlined in Fig. 13-59. The vertical and composite synchronizing signals separated from the external video signal are applied to pins 13 and 14 (VSYNC and HSYNC), and the same negative vertical and horizontal synchronizing signals as in computer mode are passed to the RGB terminal by IC109 and IC106. These synchronizing signals are thus synchronized with the external video signal. The color subcarrier (4.433618MHz) synchronized with the color synchronizing signal in the external video signal is passed from the color subcarrier oscillator to pin 17 (CKI1). The composite synchronizing signal separated from the external video signal is passed to pin 7 (EXSI). Horizontal synchronizing signal noise is removed by passing the input signal to G8, a frequency divider (1/272), and FF4. Since the pulse width of the G8 output is extremely narrow, this width is increased to about 3.5µsec by FF3. In external video and superimpose modes, the horizontal synchronizing signal frequency (pulse width approximately 3.5µsec) is obtained from pin 3(EXHP1).

The signal synchronized with the pin 3 output and applied to pin 4 is generated by the horizontal synchronizing signal processing circuit. This signal is applied to a frequency divider (1/4) in the gate array before being passed to the phase comparator as a 3.906kHz reference signal. When the external signal is the standard signal, the VCO output is 10.6785MHz and is applied to pin 29 (CKI2).

The CKI1 inverted signal passed via the counter, and the HSYNC obtained from EXSI are applied to the burst gate pulse generator, resulting in output of $\overline{BGP}$ from pin 16, BGP1 from pin 21, and BGP2 from pin 19. The LMUTE signal from the gate array (IC3) is passed to pin 22, the $\overline{CASON}$ signal from PPI (IC4) is passed to pin 31, and the RESET signal is applied to pin 27. If LMUTE is changed to H when $\overline{CASON}$ and $\overline{RST}$ are also at H, an L output is obtained from pin 32 RMUTE. And if $\overline{RST}$ is changed to L, the RMUTE output is changed to H. This circuit is used to control muting of external audio signals. Otherwise, the circuit operates in the same way as in computer mode. See Fig. Photo. 13-25 for relevant waveforms.



(a) RSYNC



(b) EXHP2

Photo 13-25

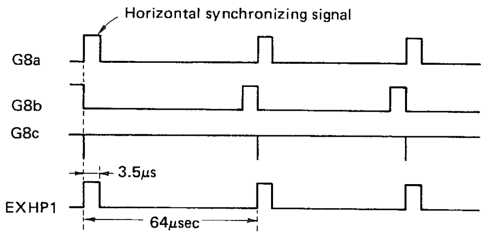


Fig. 13-58 Relevant waveforms in synthesis mode

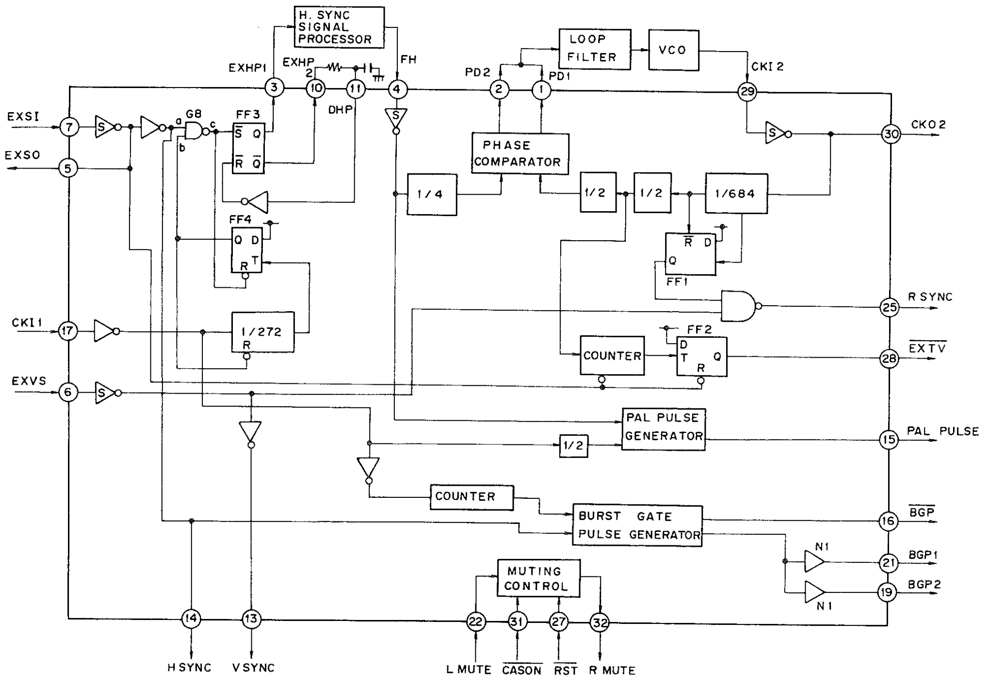


Fig. 13-59 Synchronizing pulse generator (external video and picture synthesis modes)

13. 21 RF Modulator

- Buffer 5 and clamp circuit 2

Part of the video output from the VIDEO OUT terminals is applied to the VIDEO input of the RF modulator with the front edge of the synchronizing signal clamped at 0V by Q284 and Q283.
The RF modulator input is maintained at 1Vp-p by the VIDEO connector break switch when the VIDEO OUT terminals are left open (since the video output signal is 2Vp-p), and by terminating by R293 (75 ohms) when the VIDEO OUT cable is not connected.

- Mixing/pre-emphasis circuit

The AUDIO OUT left and right channel signals are mixed as monaural signals by R360 and R361, and the high end of the signal is boosted (time constant of 50usec) by the pre-emphasis circuit consisting of Q314 and Q311. The signal is then limited (to prevent overmodulation) by the D113 and D114 diodes before being passed to the AUDIO terminals of the RF modulator.

13. 22 THROUGH Switch

- THROUGH switch function

The THROUGH switch is used to switch video and audio (left and right channel) signals to the internal circuits (NORMAL) where superimposing, sound mixing, and other processing is executed before the signals are passed to the output, or directly to the video and audio (left and right channel) outputs bypassing the internal circuits (THRU.). Since there is a number of circuits to be switched together with the power supply, a special relay with integrated plunger and switch is used.

This relay includes the equivalent of two plungers PM1 and PM2. The unit is switched to through mode when PM1 is on, and to normal mode when PM2 is on. (Needless to say, PM1 and PM2 cannot be activated simultaneously.) Also note that the plungers need to be activated by single pulses, so consecutive switching can result in the coils being burnt out.

When the power is off, the THROUGH switch is put into the THROUGH position irrespective of the video/audio switch S101 position (see Table 13-61). And when the power is switched on, the THROUGH switch is switched to NORMAL or THROUGH by S101.

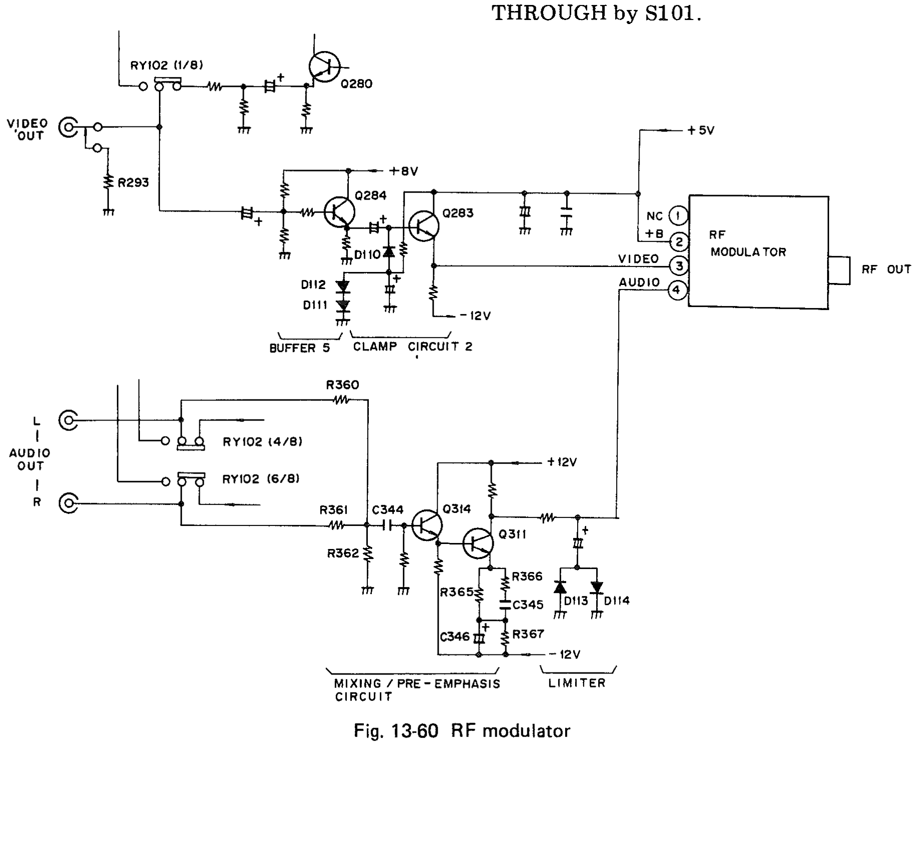


Fig. 13-60 RF modulator

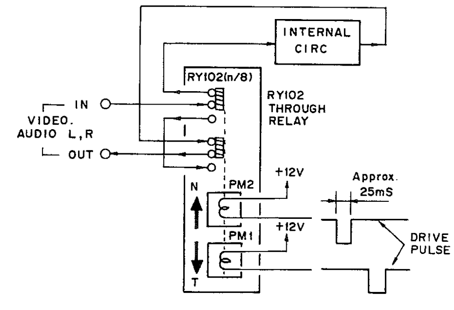


Fig. 13-61 Through switch functions

Table 13-14 Through switch position

POWER	VIDEO · AUDIO SW	POSITION
OFF	X	THROUGH
ON	NORMAL	NORMAL
	THROUGH	THROUGH

• THROUGH switch circuit

The THROUGH switch circuit consists of the THROUGH relay (RY102), a charge storage circuit (D140, D138, C406, and C421), a driver (Q401 and Q402), a switch position detector circuit (RY102(7/8), IC113(3/4), and R405), a pulse generator (IC113 (1/4, 2/4, 4/4) and delay circuit), a timing circuit (Q403, D139, R406, R407, and C402), a rectifier (D119, D118, C403, and C404), and a video/audio switch (S101). The operation of this circuit is outlined below in respect to the timing chart (see Fig. 13-63).

If the power is assumed to be switched on at time t1 with RY102 in the THROUGH position and S101 in the NORMAL position prior to time t1, an AC waveform will appear at "a", and "g" is rectified at a negative potential (about −1V) by the rectifier. Q403 is turned off, and "h" becomes the regulated power line voltage (H level) due to R408. D139 is off, and "i" is increased because of the R406/C402 time constant (where R406≫R407). When "i" reaches the IC113(3/4) threshold level (t2), "j" is changed to L, and "h" is connected to "k" since RY102 is in the THROUGH position, resulting in "k" being changed to H, and "l" to L. Therefore, "m" is also changed to L. If "j" is changed to L at t2, "n" is changed to H (since "m" is also at L), resulting in Q401 being turned on, PM2 being activated (since "p" is changed to L), and RY102 being changed to the NORMAL position. If RY102 is changed to NORMAL position at t3, "j" is connected to "k", resulting in "k" being changed to L and "l" being changed to H, thereby increasing the level of "m" (in accordance with the delay circuit). When the "m" level reaches the IC113 threshold level, "n" is changed to L, Q401 is turned off, "p" is changed to H, and the PM is switched off, thereby completing the plunger drive operation at t4. Since current is passed to PM2 from C406 during the t2 thru t4 interval, the "e" level decreases, but is increased again according to the R414/C406 time constant after t4. Since "h" is at H and "o" remains at L during this series of operations, PM1 is kept off.

If S101 is switched to the THROUGH position at t5, the current circuit is cut, and "g" is increased sharply since C403 is charged up via R413. Q403 is turned on, "h" is changed to L, D139 is turned on, and C402 is discharged, resulting in "i" being changed to L and "j" to H. Since RY102 is still in NORMAL position at this time, "k" is changed to H and "l" and "m" are changed to L, resulting in "h" and "m" being changed to L, "o" being changed to H, Q402 being turned on, and followed by PM1 also being turned on with RY102 being switched to the THROUGH position. Hence, with RY102 in THROUGH position at t6, "k" is changed to L since it is connected to "h", "l" is changed to H, and "m" is increased. When "m" reaches the IC113(2/4) threshold level, "o" is changed to L, Q402 is turned off, and PM1 is turned off to complete the plunger drive operation at t11.

If S101 is switched to NORMAL position at t8, "g" becomes negative, and the same sequence of events from t1 to t4 to switch RY102 back to NORMAL position. And if the power is switched off at t12, "a" becomes zero, "g" is increased, and RY102 is switched back to NORMAL position by the same sequence of events from t5 to t7. Due to the regulated power supply and the charge storage circuit, the switching is not effected by a reduction in the "b" level.

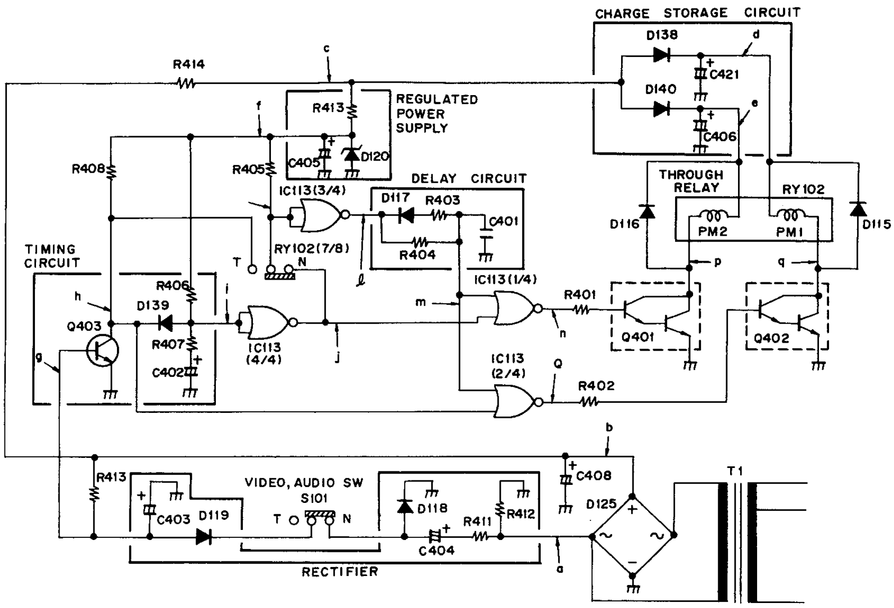


Fig. 13-62 Thorugh switch circuit

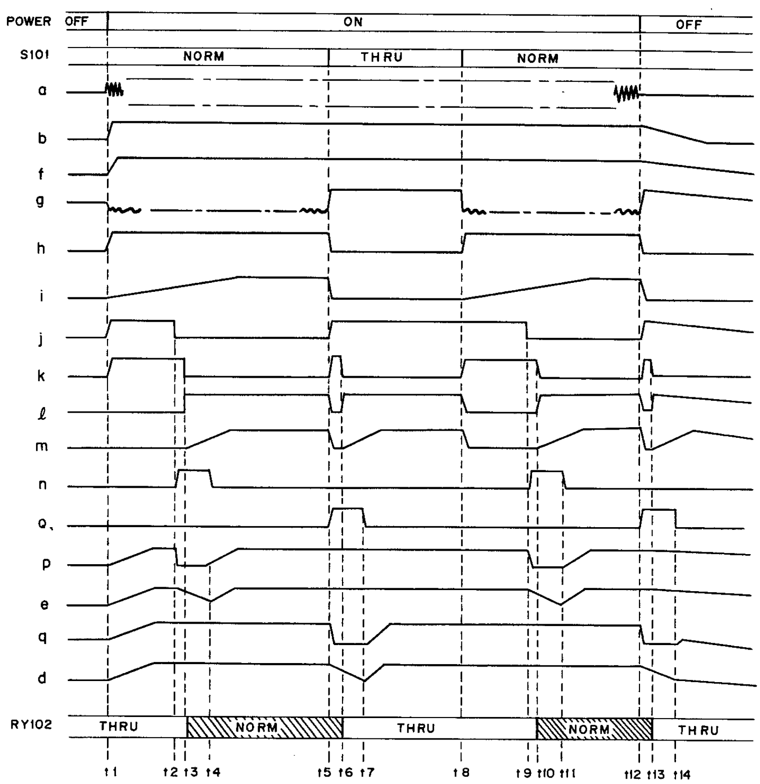


Fig. 13-63 Timing chart

13. 23 Power Supply Circuit

The PX-7 power supply circuit consists of a primary coil line filter, a power transformer (T1), and secondary coil rectifier, and a number of regulators to obtain +5V (Vcc1), +12V (Vcc2), and -12V (Vcc3).

The primary coil voltage can be switched to 220V and 240V to enable the PX-7 to be used in different regions. Inserting the T1 primary coil cable connector in J24 sets the voltage to 240V, while inserting in J25 sets the voltage to 220V. HB models have been set to 240V and HE models to 220V prior to shipment from the factory. If for some reason, however, the voltage setting needs to be changed, it will be necessary to open the bonnet and reconnect the connector described above (user servicing not permitted). While the HB model power cable has not been fitted with a plug, HE model has been fitted with the European (continental) plug. The line filter consisting of L105, C414, C415, C416, C418, C419, and C420 reduces power line noise for improved operational stability.

D127 is the power indicator LED (red), and D133 diode is inserted to prevent back current. The +5V and +12V power lines are regulated by bridge diode D125 and D126, triode regulator IC115 and IC114. The −12V line is regulated in conformity with the +12V line.

IC115 and IC114 include L-shaped current limiters for protection against overcurrent. And R418 and Q406 are used for overcurrent protection purposes in the −12V line. Note that the +5V, +12V, and −12V lines are all opened externally via the various input/output connectors to prevent damage by possible short shorting as a result of user misoperation.

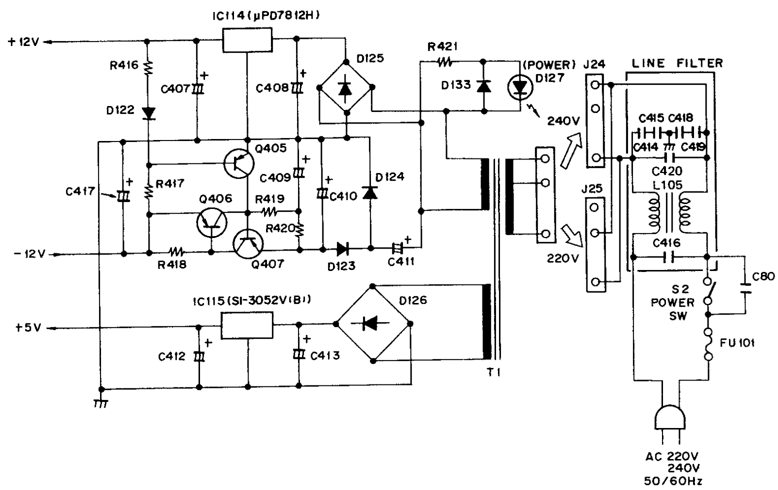


Fig. 13-64 Power supply circuit